

# BROADMOOR 15 QN20-P1 Schematics

## Tiger Lake-H

### 203061 REV:SB

<Variant Name>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A4

Document Number

**Broadmoor 15 TGL-H**

Rev  
**X01**

Date: Monday, October 26, 2020

Sheet 1 of 106



63	SSD2_PCIE_RX_N1	《 》	63	SSD2_PCIE_RX_N3	《 》
63	SSD2_PCIE_RX_P1	《 》	63	SSD2_PCIE_RX_P3	《 》
63	SSD2_PCIE_TX_N1	《 》	63	SSD2_PCIE_TX_N3	《 》
63	SSD2_PCIE_TX_P1	《 》	63	SSD2_PCIE_TX_P3	《 》
63	SSD2_PCIE_RX_N2	《 》	63	SSD2_PCIE_RX_N0	《 》
63	SSD2_PCIE_RX_P2	《 》	63	SSD2_PCIE_RX_P0	《 》
63	SSD2_PCIE_TX_N2	《 》	63	SSD2_PCIE_TX_N0	《 》
63	SSD2_PCIE_TX_P2	《 》	63	SSD2_PCIE_TX_P0	《 》

16	DMI_RX_CPU_P7	16	DMI_TX_CPU_P7
16	DMI_RX_CPU_N7	16	DMI_TX_CPU_N7
16	DMI_RX_CPU_P6	16	DMI_TX_CPU_P6
16	DMI_RX_CPU_N6	16	DMI_TX_CPU_N6
16	DMI_RX_CPU_P5	16	DMI_TX_CPU_P5
16	DMI_RX_CPU_N5	16	DMI_TX_CPU_N5
16	DMI_RX_CPU_P4	16	DMI_TX_CPU_P4
16	DMI_RX_CPU_N4	16	DMI_TX_CPU_N4
16	DMI_RX_CPU_P3	16	DMI_TX_CPU_P3
16	DMI_RX_CPU_N3	16	DMI_TX_CPU_N3
16	DMI_RX_CPU_P2	16	DMI_TX_CPU_P2
16	DMI_RX_CPU_N2	16	DMI_TX_CPU_N2
16	DMI_RX_CPU_P1	16	DMI_TX_CPU_P1
16	DMI_RX_CPU_N1	16	DMI_TX_CPU_N1
16	DMI_RX_CPU_P0	16	DMI_TX_CPU_P0
16	DMI_RX_CPU_N0	16	DMI_TX_CPU_N0

```

76 GFX PCIE RX P7
76 GFX PCIE RX P7
76 GFX PCIE RX P6
76 GFX PCIE RX N6
76 GFX PCIE RX P5
76 GFX PCIE RX N5
76 GFX PCIE RX P4
76 GFX PCIE RX N4
76 GFX PCIE RX P3
76 GFX PCIE RX N3
76 GFX PCIE RX P2
76 GFX PCIE RX N2
76 GFX PCIE RX P1
76 GFX PCIE RX N1
76 GFX PCIE RX P0
76 GFX PCIE RX N0

```

76	GFX_PCIE_TX_CON_P7	
76	GFX_PCIE_TX_CON_N7	
76	GFX_PCIE_TX_CON_P6	
76	GFX_PCIE_TX_CON_N6	
76	GFX_PCIE_TX_CON_P5	
76	GFX_PCIE_TX_CON_N5	
76	GFX_PCIE_TX_CON_P4	
76	GFX_PCIE_TX_CON_N4	

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76 GFX_PCIE_TX_CON_P3
76 GFX_PCIE_TX_CON_N3
76 GFX_PCIE_TX_CON_P2
76 GFX_PCIE_TX_CON_N2
76 GFX_PCIE_TX_CON_P1
76 GFX_PCIE_TX_CON_N1
76 GFX_PCIE_TX_CON_P0
76 GFX_PCIE_TX_CON_N0

```

SSD2\_PCIE\_RX\_P3  
SSD2\_PCIE\_RX\_N3  
SSD2\_PCIE\_RX\_P2  
SSD2\_PCIE\_RX\_N2  
SSD2\_PCIE\_RX\_P1  
SSD2\_PCIE\_RX\_N1  
SSD2\_PCIE\_RX\_P0  
SSD2\_PCIE\_RX\_N0

N15	PCIE16_RX_P_15
M15	PCIE16_RX_N_15
J15	PCIE16_RX_P_14
K15	PCIE16_RX_N_14
M17	PCIE16_RX_P_13
L17	PCIE16_RX_N_13
H17	PCIE16_RX_P_12
J17	PCIE16_RX_N_12
N18	PCIE16_RX_P_11
M18	PCIE16_RX_N_11
J18	PCIE16_RX_P_10
K18	PCIE16_RX_N_10
M20	PCIE16_RX_P_9
L20	PCIE16_RX_N_9
H20	PCIE16_RX_P_8
J20	PCIE16_RX_N_8
N22	PCIE16_RX_P_7

GFX\_PCIE\_RX\_P7  
GFX\_PCIE\_RX\_N7  
GFX\_PCIE\_RX\_P6  
GFX\_PCIE\_RX\_N6  
GFX\_PCIE\_RX\_P5  
GFX\_PCIE\_RX\_N5  
GFX\_PCIE\_RX\_P4  
GFX\_PCIE\_RX\_N4  
GFX\_PCIE\_RX\_P3  
GFX\_PCIE\_RX\_N3  
GFX\_PCIE\_RX\_P2  
GFX\_PCIE\_RX\_N2  
GFX\_PCIE\_RX\_P1  
GFX\_PCIE\_RX\_N1  
GFX\_PCIE\_RX\_P0  
GFX\_PCIE\_RX\_N0

X C41	RSVD_TP_9
X D41	RSVD_TP_10
X A40	RSVD_TP_11
X B40	RSVD_TP_12

R303 1 2 2K2R2F-GP DMI\_RCOMP\_P  
DMI\_RCOMP\_N

DMI TX CPU P7
DMI TX CPU_N7
DMI TX CPU_P6
DMI TX CPU_N6
DMI TX CPU_P5
DMI TX CPU_N5
DMI TX CPU_P4
DMI TX CPU_N4
DMI TX CPU_P3
DMI TX CPU_N3
DMI TX CPU_P2
DMI TX CPU_N2
DMI TX CPU_P1
DMI TX CPU_N1
DMI TX CPU_P0
DMI TX CPU_N0

 B3  
 B4

RSVD\_TP\_13  
 RSVD\_TP\_14

TIGER-LAKE-H-1-GP-U3

3 OF 15

```
PCIE4_TX_P_3
PCIE4_TX_N_3
PCIE4_TX_P_2
PCIE4_TX_N_2
PCIE4_TX_P_1
PCIE4_TX_N_1
PCIE4_TX_P_0
PCIE4_TX_N_0
```

PCIE16_TX_P_15	E16
PCIE16_TX_N_15	D16
PCIE16_TX_P_14	A16
PCIE16_TX_N_14	B16
PCIE16_TX_P_13	F17
PCIE16_TX_N_13	E17
PCIE16_TX_P_12	B17
PCIE16_TX_N_12	C17
PCIE16_TX_P_11	E18
PCIE16_TX_N_11	D18
PCIE16_TX_P_10	A18
PCIE16_TX_N_10	B18
PCIE16_TX_N_10	F20
PCIE16_TX_P_9	E20
PCIE16_TX_N_9	B20
PCIE16_TX_P_8	C20
PCIE16_TX_N_8	E22

E28	SSD2_PCIE_TX_P3
D28	SSD2_PCIE_TX_N3
A28	SSD2_PCIE_TX_P2
B28	SSD2_PCIE_TX_N2
F29	SSD2_PCIE_TX_P1
E29	SSD2_PCIE_TX_N1
B29	SSD2_PCIE_TX_P0
C29	SSD2_PCIE_TX_N0

E16	
D16	→
A16	→
B16	→
F17	→
E17	→
B17	→
C17	→
E18	→
D18	→
A18	→
B18	→
F20	→
E20	→
B20	→
C20	→
E22	→

PCIE16_TX_N_8	D20	GFX	PCIE_TX_P7	C3331	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P7
PCIE16_TX_P_7	D22	GFX	PCIE_TX_N7	C3324	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P7
PCIE16_TX_N_7	A22	GFX	PCIE_TX_P6	C3321	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P6
PCIE16_TX_P_6	B22	GFX	PCIE_TX_N6	C3322	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P6
PCIE16_TX_N_6	F23	GFX	PCIE_TX_P5	C3318	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P5
PCIE16_TX_P_5	B25	GFX	PCIE_TX_N5	C3320	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P5
PCIE16_TX_N_5	B23	GFX	PCIE_TX_P4	C3307	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P4
PCIE16_TX_P_4	C23	GFX	PCIE_TX_N4	C3316	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P4
PCIE16_TX_N_4	E25	GFX	PCIE_TX_P3	C3314	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P3
PCIE16_TX_P_3	D25	GFX	PCIE_TX_N3	C3304	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P3
PCIE16_TX_N_3	B25	GFX	PCIE_TX_P2	C3313	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P2
PCIE16_TX_P_2	B25	GFX	PCIE_TX_N2	C3313	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P2
PCIE16_TX_N_2	F27	GFX	PCIE_TX_P1	C3312	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P1
PCIE16_TX_P_1	E27	GFX	PCIE_TX_N1	C3302	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P1
PCIE16_TX_N_1	B27	GFX	PCIE_TX_P0	C3310	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P0
PCIE16_TX_P_0	C27	GFX	PCIE_TX_N0	C3311	SC022U10V2KX-2-GP	GFX	PCIE_TX_CON_P0

Signal	Pin	Function	Pin	Function	Pin	Function
PCIE16_COM0_RCOMP_P	U11	PCIE16_RCOMP_P	R301	1	2	2K2R2F-GP
PCIE16_COM0_RCOMP#	R11	PCIE16_RCOMP_N				
PCIE4_RCOMP_P	T26	PCIE4_RCOMP_P	R302	1	2	2K2R2F-GP
PCIE4_RCOMP#	R26	PCIE4_RCOMP_N				

DMI_TX_N_7	H13	DMI_RX_CPU_N7
DMI_TX_P_6	M13	DMI_RX_CPU_P6
DMI_TX_N_6	L13	DMI_RX_CPU_N6
DMI_TX_P_5	H11	DMI_RX_CPU_P5
DMI_TX_N_5	G11	DMI_RX_CPU_N5
DMI_TX_P_4	N11	DMI_RX_CPU_P4
DMI_TX_N_4	L11	DMI_RX_CPU_N4
DMI_TX_P_3	E10	DMI_RX_CPU_P3
DMI_TX_N_3	D10	DMI_RX_CPU_N3
DMI_TX_P_2	F9	DMI_RX_CPU_P2
DMI_TX_N_2	E8	DMI_RX_CPU_N2
DMI_TX_P_1	E9	DMI_RX_CPU_P1
DMI_TX_N_1	D8	DMI_RX_CPU_N1
DMI_TX_P_0	D6	DMI_RX_CPU_P0
DMI_TX_N_0	C6	DMI_RX_CPU_N0

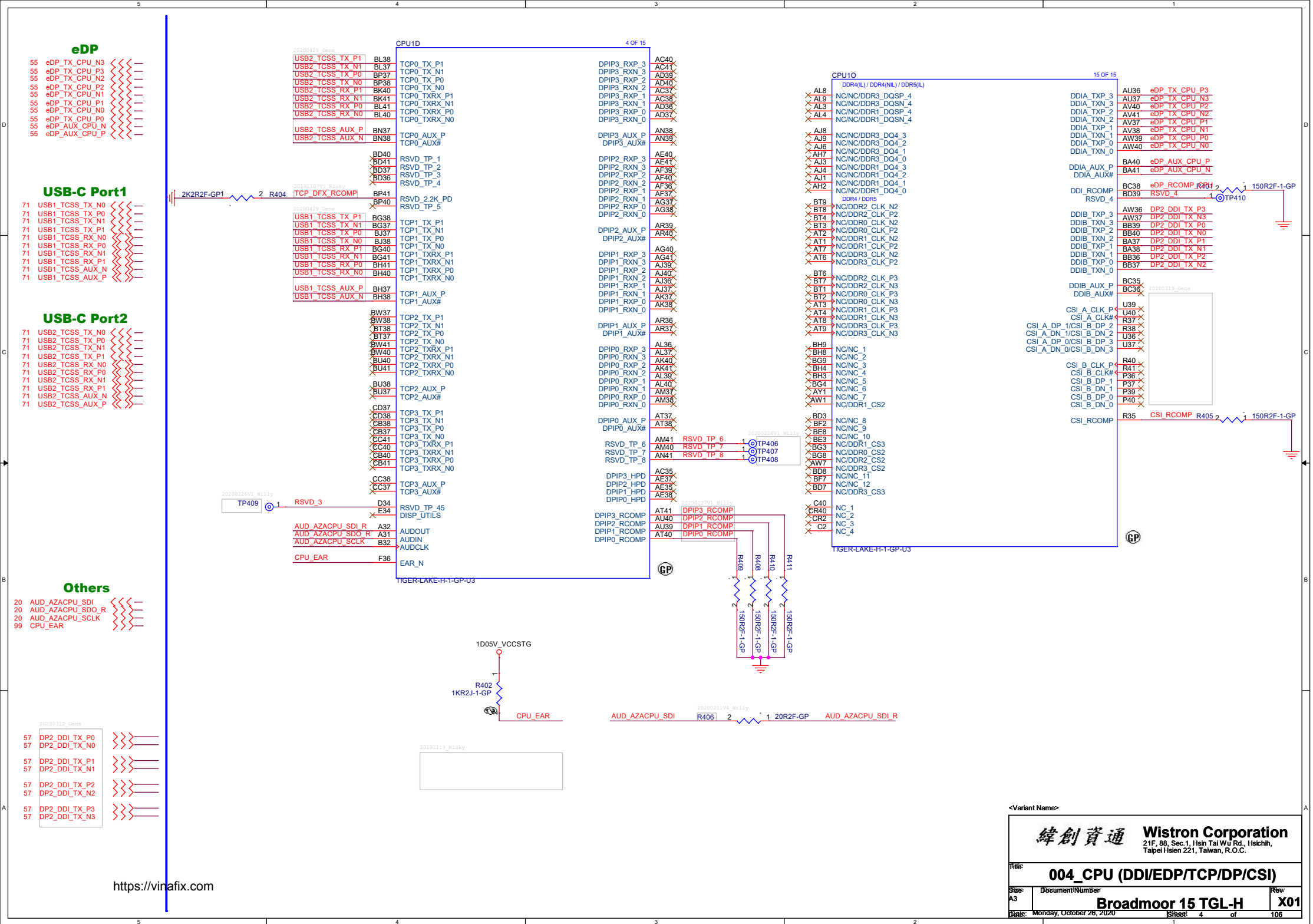


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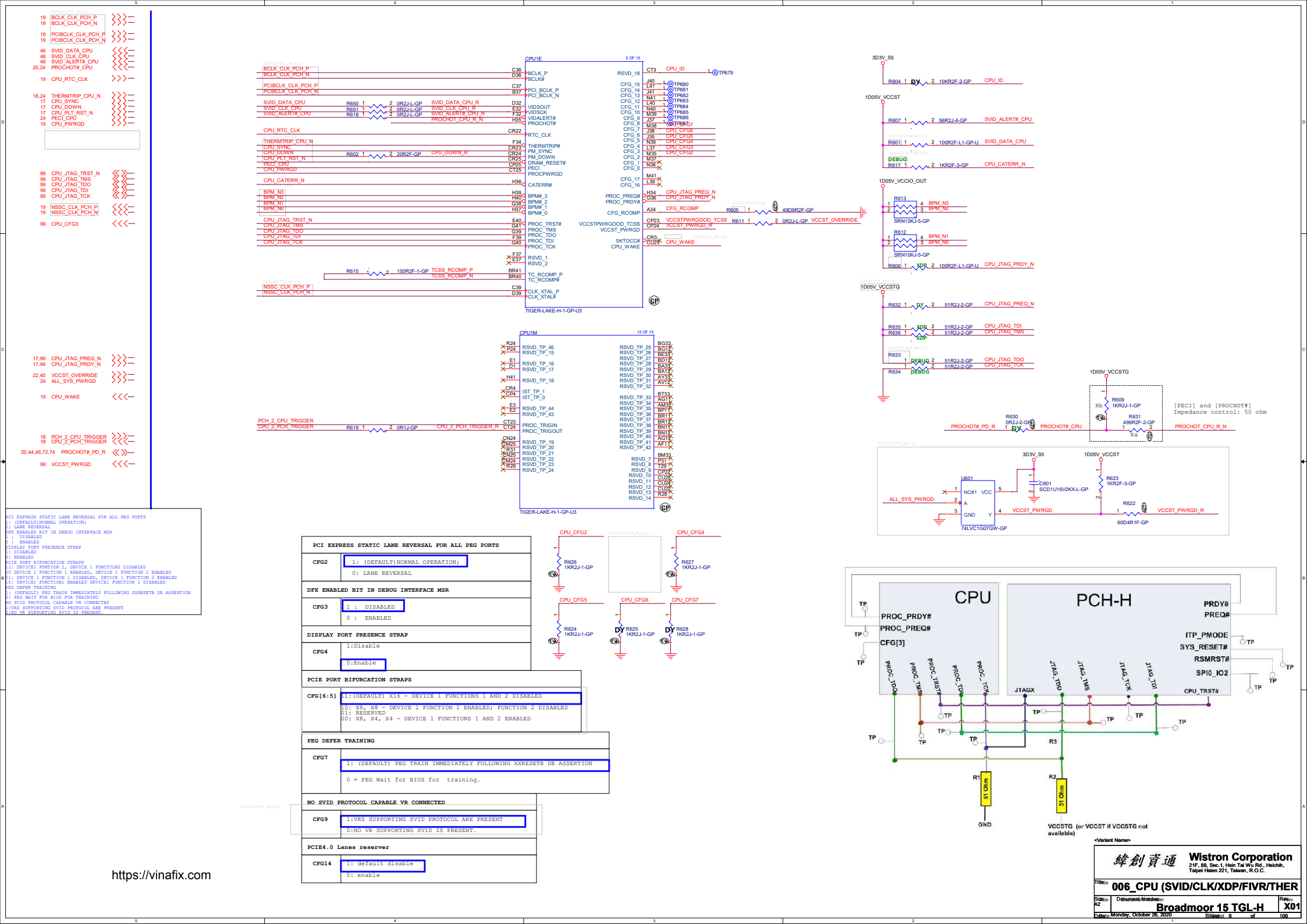
Title	003_CPU (PEG/DMI/PCIE4.0)
-------	---------------------------

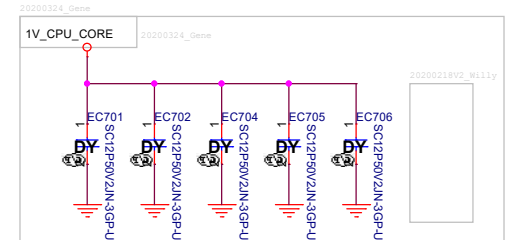
Size: A3	Document Number: <b>Broadmoor 15 TGL-H</b>	Rev: <b>X01</b>
Date: Monday, October 26, 2020	Sheet: 3 of	106

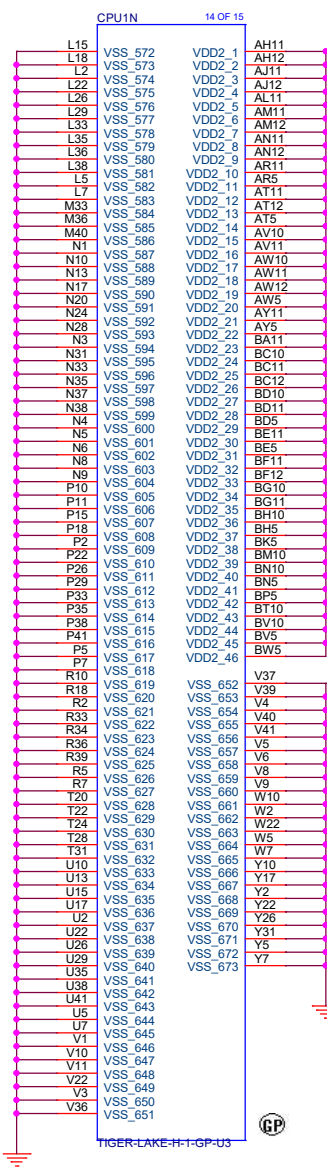
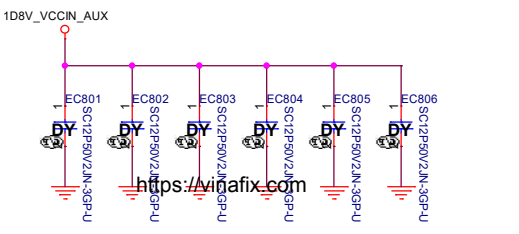
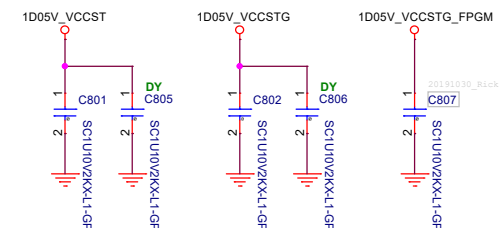
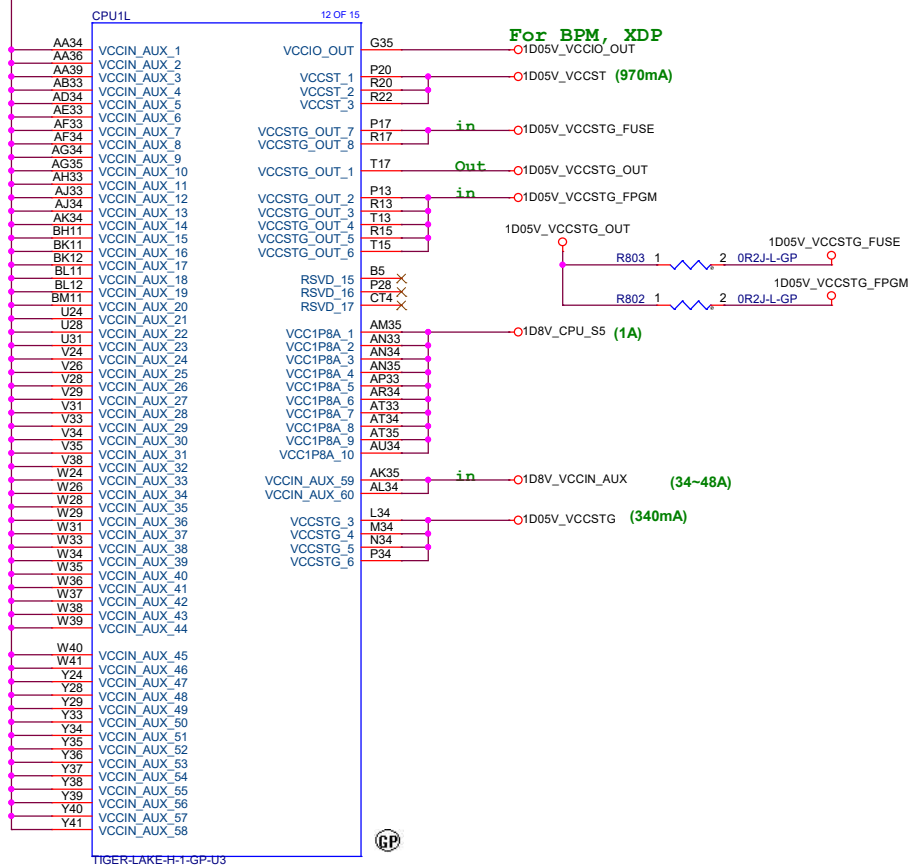




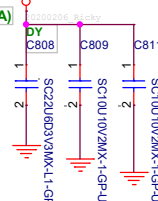
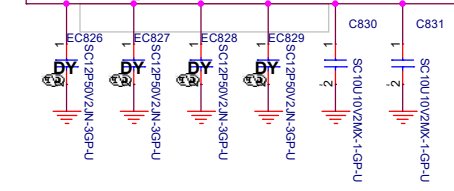
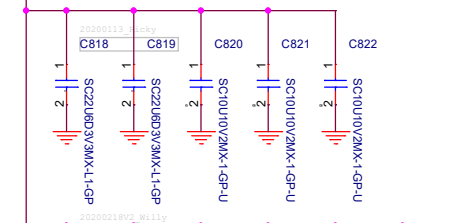
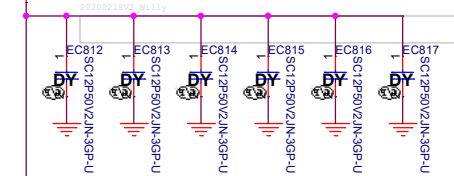






(22~42A)  
1D8V\_VCCIN\_AUX20200324\_Gene  
1D2V\_S3 (4.3A)

1D8V\_CPU\_S5 (2A)

20200324\_Gene  
1D2V\_S3

Power Rail	Decap Placement	Form Factor	Value	Number
VDD2	Secondary Side	0603	22uF	2
		0402	10uF	1
		0402	Place Holder	2

&lt;Variant Name&gt;

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Title

008\_CPU (VCCIN\_AUX/VCCST/VCCSTG

Size

Document Number

A3

Broadmoor 15 TGL-H

Date: Monday, October 26, 2020

Sheet

8

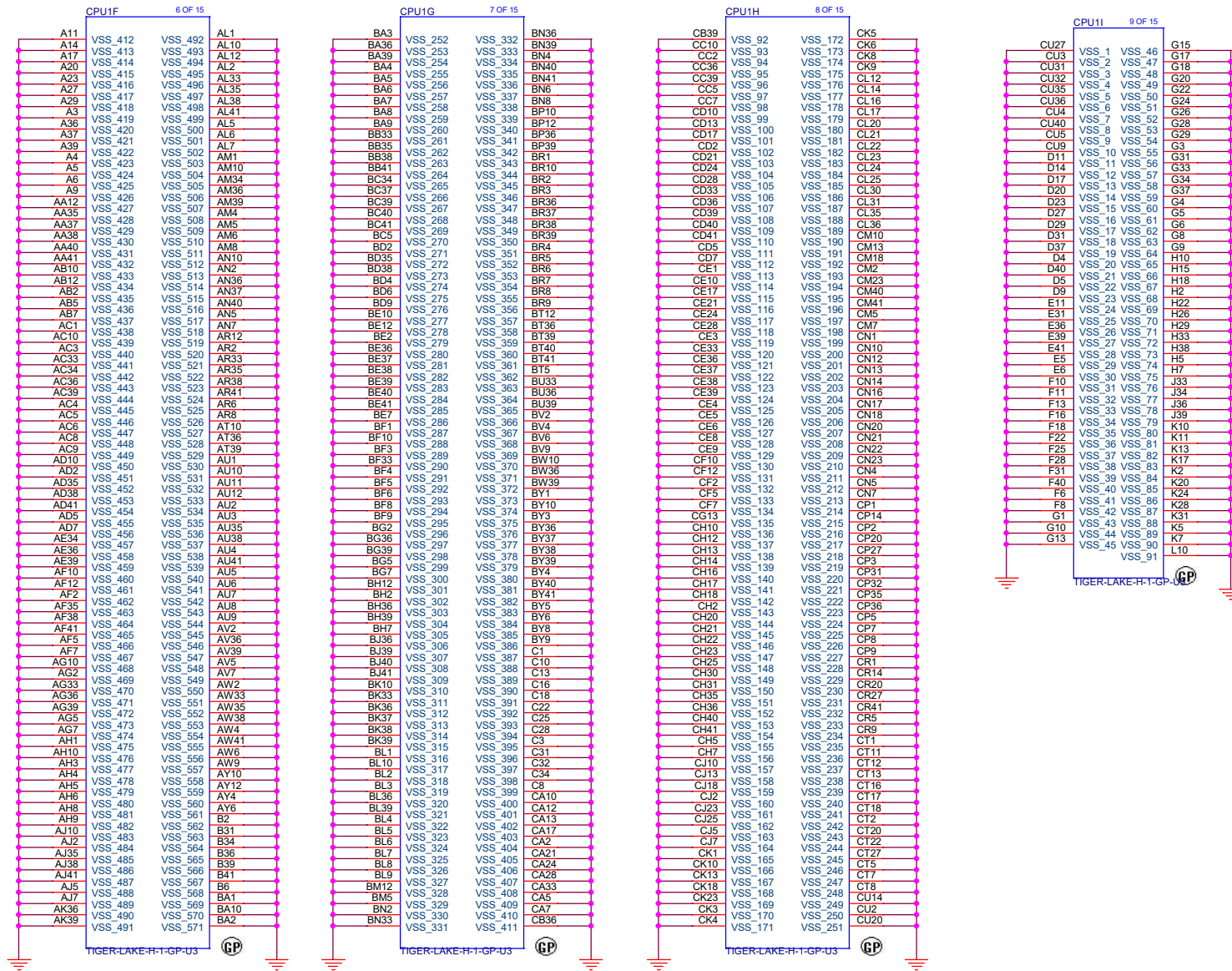
of

106

Rev

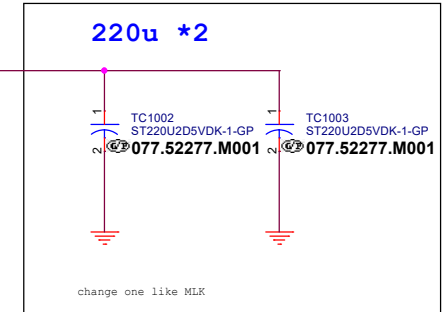
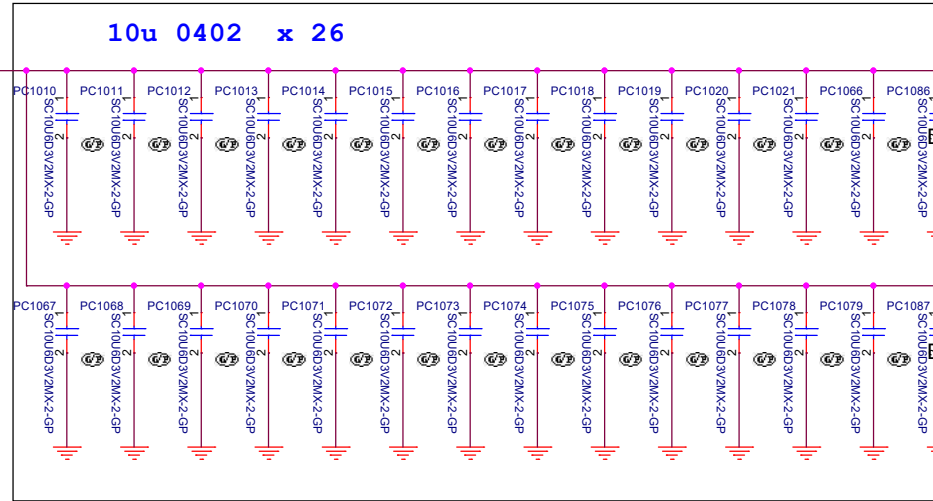
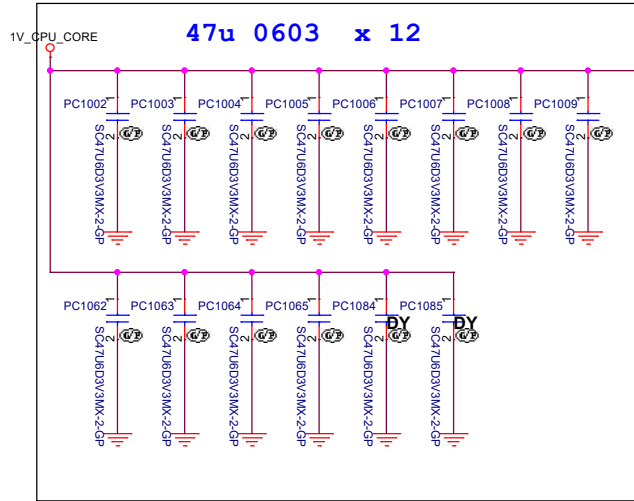
X01



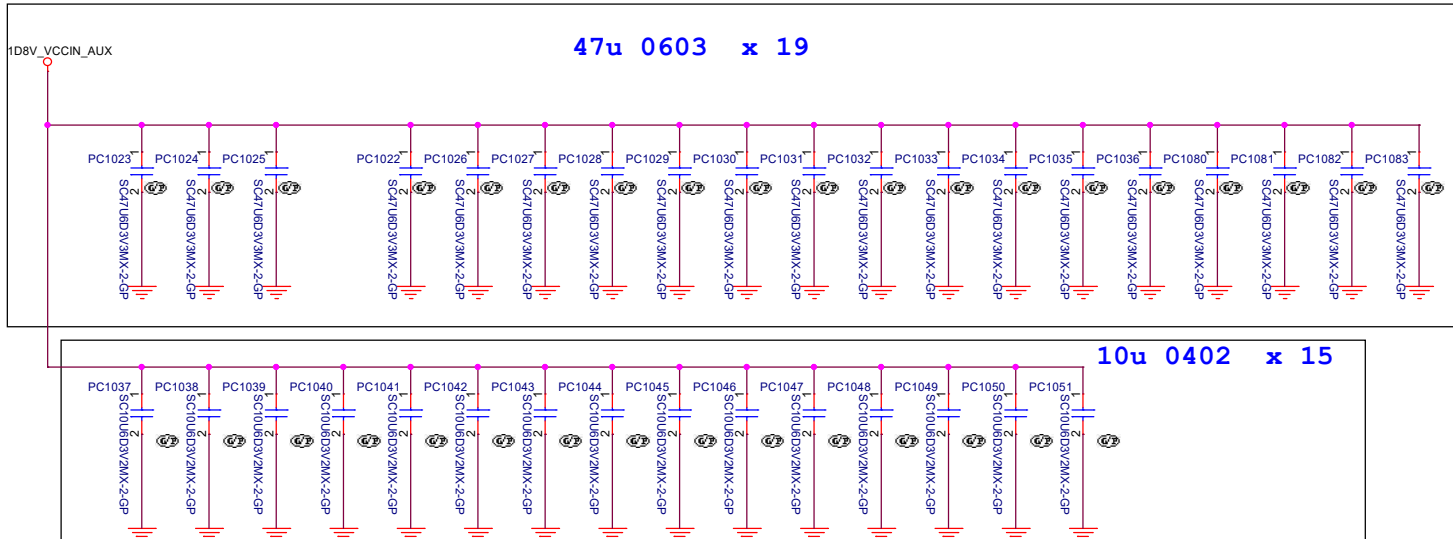


# Main Func = CPU

## 1V\_CPU\_CORE (VCCIN)



## VCCIN\_AUX



Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN	Primary Side	7343	220uF (7mΩ ESR)	4
		7343	PlaceHolder	2
	Secondary Side	0603	47uF	10
		0603	PlaceHolder	2
		0402	10uF	25
		0402	PlaceHolder	2

Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX	CPU Primary Side	7343	330uF	2
		0603	47uF	4
	CPU Secondary side	0402	10uF	6
		0603	47uF	8
	PCH Primary Side	0603	47uF	5
		0402	10uF	4

18.68 SPI\_SI\_CPU <<<-  
18.68 SPI\_WP\_CPU <<>-  
18.68 SPI\_HOLD\_CPU <<>-  
21 HDA\_SDOUT <<<-  
21.61 CNV\_RGI\_DT >>>-  
21 JTAG\_ODT\_EN <<<-  
20.71 TBT\_LSX0\_RXD >>>-  
20.71 TBT\_LSX1\_RXD <<<-  
20.99 DBG\_FMODE <<<-  
21.61 CNV\_BRI\_DT <<<-  
16.71 PCH\_TBT\_PERST# >>>-  
21 TPM\_IDENTIFY <<<-  
20.24.27 SPKR <<<-  
21 IA\_BASELINE\_SEL <<<-

GPIO	GPP_C5 eSPI Disable	SPIO_MOSI Reserved	GPP_H15 JTAG ODT Disable	GPP_J2 XTAL Freq Selection	SPI_IO_2 SPI_WP_CPU	GPP_R2 / HDA_SDO Flash Security Override	GPP_J4 / CNV_RGI_DT M.2 CNV1 Debug Mode Select	GPP_E6/SATA_DEVSLP2
Schematic								
High	Disable eSPI.	Reserved	JTAG ODT is enabled	24 MHz	Reserved	Disable Flash Descriptor Security	INTEGRATED CNVI DISABLE	High for ST Micro
Low	Enable eSPI =default=	Reserved	JTAG ODT is disabled	38.4 MHz =default=	Reserved	Enable Flash Descriptor security measures	INTEGRATED CNVI ENABLE	Low for Nuvoton.
GPIO	GPP_G13 TBT_LSX0_VCC config	GPP_G15 TBT_LSX1_VCC config	GPP_G14 TBT_LSX2_VCC config	GPP_G11 TBT_LSX3_VCC config	SPI_IO_3 SPI_HOLD_CPU	DBG_FMODE	GPP_B18 No Reboot	GPD_7 Reserved
Schematic								
High	DDP1 I2C/TBT_LSX0/BSSB_LSO pins at 3.3V	DDP2 I2C/TBT_LSX1/BSSB_LSO pins at 3.3V	3.3V	3.3V	Reserved	DPXTESTMODE DISABLED (DEFAULT)	Enable "No Reboot" mode	Reserved
Low	DDP1 I2C/TBT_LSX0/BSSB_LSO pins at 1.8V	DDP2 I2C/TBT_LSX1/BSSB_LSO pins at 1.8V	1.8V	1.8V	Reserved	DPXTESTMODE ENABLED	Disable "No Reboot" mode	Reserved
GPIO	GPP_B14/SPKR	GPP_K4						
High	3.3V							
Low	1.8V							
								XTAL INPUT MODE HIGH : XTAL INPUT IS SINGLE ENDED LOW : XTAL IS ATTACHED

#### Original Ref.

GPP_C5	SPIO_MOSI	GPP_H15 / SML3ALERT#	GPP_J2/ CNV_BRI_DT	SPIO_IO2	GPP_R2 / HDA_SDO	GPP_J4/ CNV_RGI_DT	GPP_G13/ TBT_LSX0_VCC config	GPP_G15/ TBT_LSX1_VCC config	GPP_G9/ TBT_LSX2_VCC config
GPP_G11/ TBT_LSX3_VCC config	SPIO_IO3	DBG_FMODE	GPP_B18/ GSPT0_MOSI	GPD7	GPP_B14 / SPKR	GPP_C2/ SML2ALERT#	GPP_B23/ SML1ALERT#	GPP_H12/ SML2ALERT#	GPP_B22/ GSPT1_MOSI

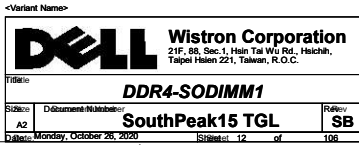
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Close DIMM1 (p.12)





5

4

3

2

1

D

D

C

C

B

B

A

A

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Title <div>014_DDR (RSVD) (DDR4-CHA1)</div>		
Size <div>A4</div>	Document Number <div>Broadmoor 15 TGL-H</div>	Rev <div>X01</div>
Date: Monday, October 26, 2020		Sheet 14 of 106

5

4

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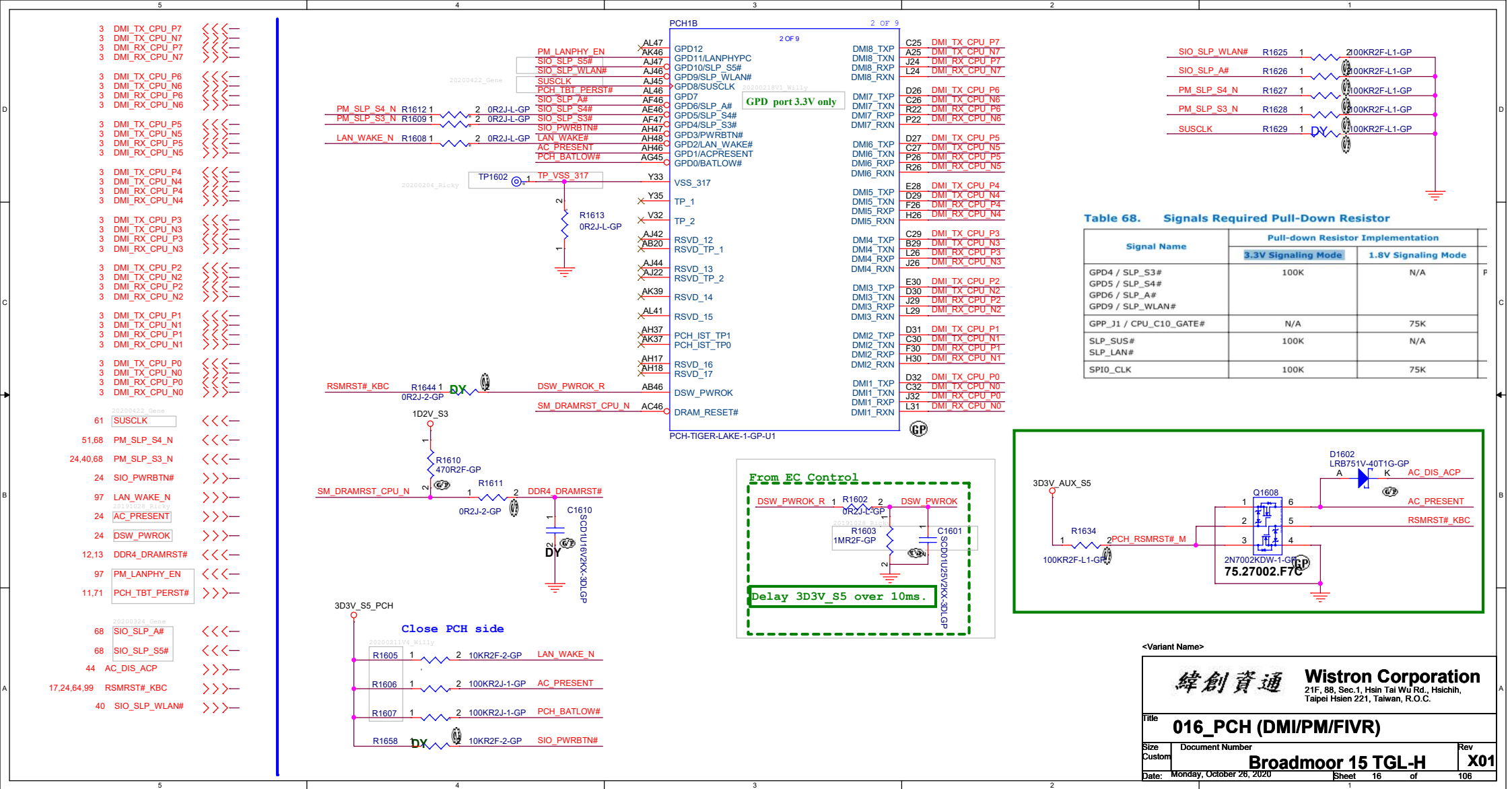
1

5	4	3	2	1
D				
C				
B				
A				

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Title015_DDR (RSVD) (DDR4-CHB1)		
SizeA4	Document NumberBroadmoor 15 TGL-H	RevX01
Date: Monday, October 26, 2020	Sheet 15	of 106



## WLAN

61 WLAN\_PCIE\_TX\_P <<<-  
61 WLAN\_PCIE\_TX\_N >>>-  
61 WLAN\_PCIE\_RX\_P <<<-  
61 WLAN\_PCIE\_RX\_N >>>-

## SSD1

63 SSD\_PCIE\_RX\_N1 <<<-  
63 SSD\_PCIE\_RX\_P1 >>>-  
63 SSD\_PCIE\_TX\_N1 <<<-  
63 SSD\_PCIE\_TX\_P1 >>>-

63 SSD\_PCIE\_RX\_N2 <<<-  
63 SSD\_PCIE\_RX\_P2 >>>-  
63 SSD\_PCIE\_TX\_N2 <<<-  
63 SSD\_PCIE\_TX\_P2 >>>-

63 SSD\_PCIE\_RX\_N3 <<<-  
63 SSD\_PCIE\_RX\_P3 >>>-  
63 SSD\_PCIE\_TX\_N3 <<<-  
63 SSD\_PCIE\_TX\_P3 >>>-

63 SSD\_SATA\_RX\_N <<<-  
63 SSD\_SATA\_RX\_P >>>-  
63 SSD\_SATA\_TX\_N <<<-  
63 SSD\_SATA\_TX\_P >>>-

## LAN

97 LAN\_PCIE\_TX\_P <<<-  
97 LAN\_PCIE\_TX\_N >>>-  
97 LAN\_PCIE\_RX\_P <<<-  
97 LAN\_PCIE\_RX\_N >>>-

6.99 CPU\_JTAG\_PRDY\_N <<<-  
6.99 CPU\_JTAG\_FREQ\_N <<<-

6 CPU\_SYNC <<<-

6 CPU\_DOWN <<<-

6 CPU\_PLT\_RST\_N <<<-

24 PCH\_PCH <<<-

40.44 PCH\_PWROK >>>-

16.24.64.99 RSMRST#\_KBC <<<-

24 RTORST\_ON <<<-  
68 RTC\_RST\_N <<<-

## WWAN

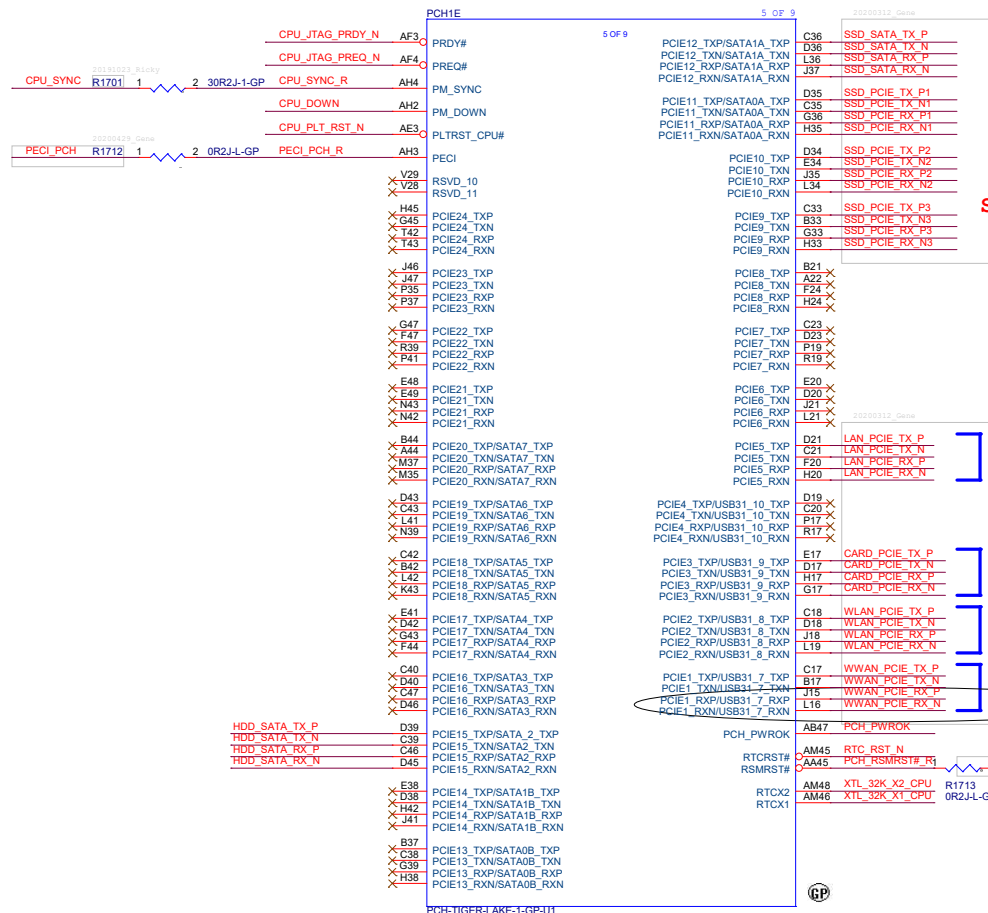
62 WWAN\_PCIE\_RX\_N <<<-  
62 WWAN\_PCIE\_RX\_P >>>-  
62 WWAN\_PCIE\_TX\_N <<<-  
62 WWAN\_PCIE\_TX\_P >>>-

## SD

33 CARD\_PCIE\_RX\_N <<<-  
33 CARD\_PCIE\_RX\_P >>>-  
33 CARD\_PCIE\_TX\_N <<<-  
33 CARD\_PCIE\_TX\_P >>>-

## HDD

60 HDD\_SATA\_TX\_P >>>-  
60 HDD\_SATA\_TX\_N <<<-  
60 HDD\_SATA\_RX\_P <<<-  
60 HDD\_SATA\_RX\_N >>>-



M.2 SSD1

SWAP P1 & P3

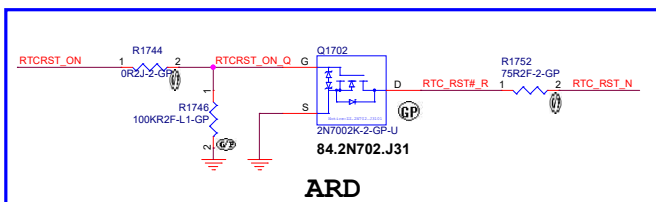
LAN

SD card

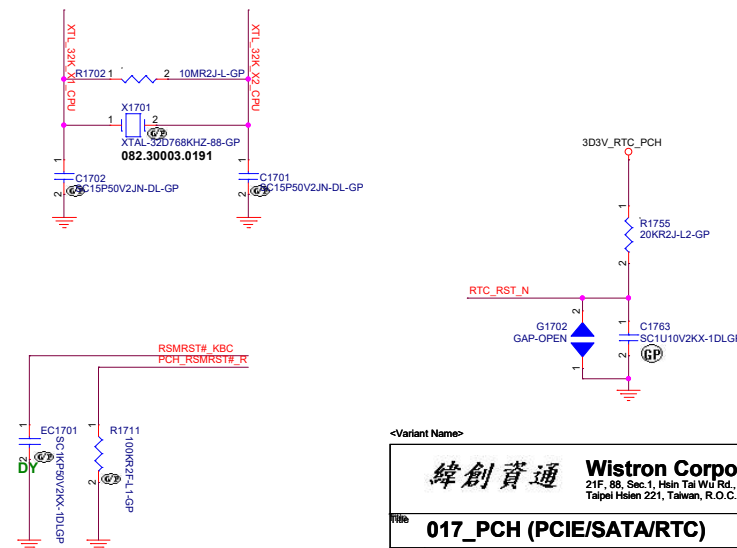
WLAN

WWAN

CHECK SP15 Function



ARD



<Variant Name>

緯創資通

Wistron Corporation  
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

File 017\_PCH (PCIE/SATA/RTC)

Size Custom Document Number Broadmoor 15 TGL-H New X01  
Date: Monday, October 26, 2020 Sheet 17 of 106

<https://vinafix.com>

## USB31

35 USB1\_USB31\_TX\_P <<<=  
35 USB1\_USB31\_TX\_N <<<=  
35 USB1\_USB31\_RX\_P <<<=  
35 USB1\_USB31\_RX\_N <<<=

35 USB2\_USB31\_TX\_P <<<=  
35 USB2\_USB31\_TX\_N <<<=  
35 USB2\_USB31\_RX\_P <<<=  
35 USB2\_USB31\_RX\_N <<<=

## USB2

73 USB1\_USB20\_P <<<=  
73 USB1\_USB20\_N <<<=

36 Charger\_USB20\_N <<<=  
36 Charger\_USB20\_P <<<=

56 CCD\_USB20\_P <<<=  
56 CCD\_USB20\_N <<<=

61 BT\_USB20\_P <<<=  
61 BT\_USB20\_N <<<=

73 USB2\_USB20\_P <<<=  
73 USB2\_USB20\_N <<<=

35 USB4\_USB20\_P <<<=  
35 USB4\_USB20\_N <<<=

## Others

6.24 THERMTRIP\_CPU\_N <<<=  
6 PCH\_2\_CPU\_TRIGGER >>>=  
6 CPU\_2\_PCH\_TRIGGER <<<=  
68 SPI\_CS\_CPU\_N1 <<<=  
18.91.96 SPI\_CS\_CPU\_N2 <<<=  
53 PM\_SLP\_SUS\_N <<<=  
40 PM\_SLP\_LAN\_N <<<=  
18.68.96 SPI\_SO\_CPU >>>=  
11.68 SPI\_SI\_CPU <<<=  
11.68 SPI\_HOLD\_CPU <<<=  
11.68 SPI\_WP\_CPU <<<=  
18.68.96 SPI\_CS\_CPU\_N0 <<<=  
18.68.96 SPI\_CLK\_CPU <<<=  
68 SYS\_RESET\_N >>>=  
24 SYS\_PWROK\_R >>>=  
24.62 PCH\_PCIE\_WAKE# <<<=  
20200217V3\_Willy

## WWAN

62 WWAN\_USB31\_RX\_N <<<=  
62 WWAN\_USB31\_RX\_P <<<=  
62 WWAN\_USB31\_TX\_N <<<=  
62 WWAN\_USB31\_TX\_P <<<=

## WWAN

62 WWAN\_USB20\_N <<<=  
62 WWAN\_USB20\_P <<<=

## USH

66 USH\_USB20\_N <<<=  
66 USH\_USB20\_P <<<=

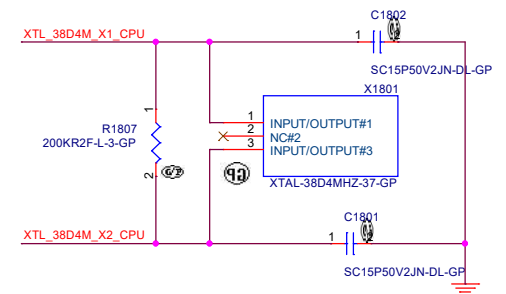
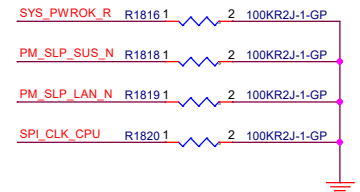
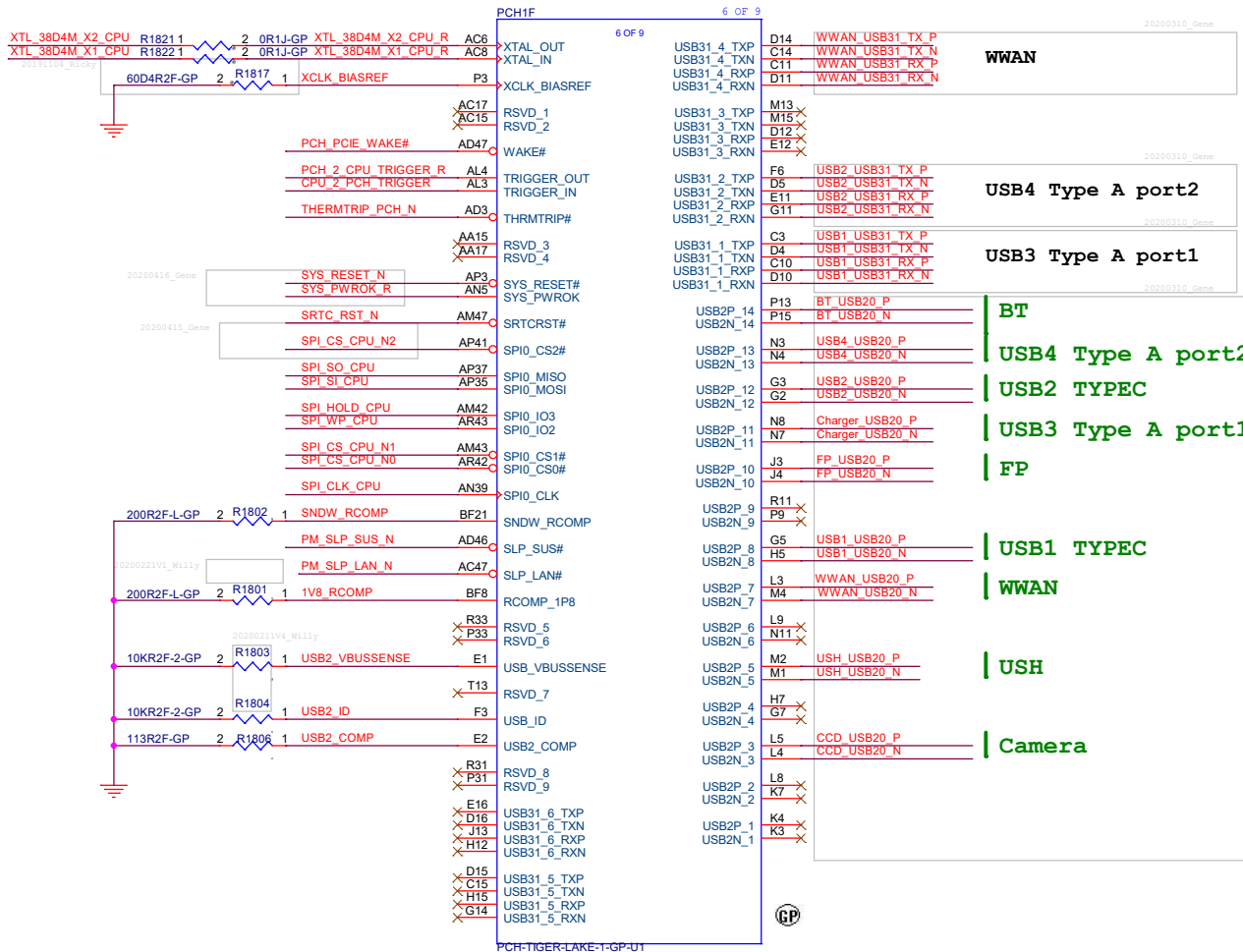
## FPR

92 FP\_USB20\_P <<<=  
92 FP\_USB20\_N <<<=

Close PCH1(p.18)

<https://vinafix.com>

18.68.96 SPI\_CLK\_CPU <<<=  
18.68.96 SPI\_SO\_CPU <<<=  
18.68.96 SPI\_CS\_CPU\_N0 <<<=  
18.91.96 SPI\_CS\_CPU\_N2 <<<=



<Variant Name>

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

Title			
018_PCH (USB31/USB2/SPI/XTAL)			
Size	Document Number	Rev	
A3	Broadmoor 15 TGL-H	X01	
Date:	Monday, October 26, 2020	Sheet	18 of 106



## SSD

63 SSD2\_CLK\_CPU\_P <<<<—  
63 SSD2\_CLK\_CPU\_N <<<<—  
63 SSD\_CLK\_CPU\_P >>>>—  
63 SSD\_CLK\_CPU\_N >>>>—

## GFX

76 GFX\_CLK\_CPU\_P >>>>—  
76 GFX\_CLK\_CPU\_N >>>>—

## LAN

97 LAN\_CLK\_CPU\_P >>>>—  
97 LAN\_CLK\_CPU\_N >>>>—

## WLAN

61 WLAN\_CLK\_CPU\_P >>>>—  
61 WLAN\_CLK\_CPU\_N >>>>—

## CNVi

61 CNV\_WT\_DP1 <<<<—  
61 CNV\_WT\_DN1 <<<<—  
61 CNV\_WT\_DP0 <<<<—  
61 CNV\_WT\_DN0 <<<<—  
61 CNV\_WT\_CLKP <<<<—  
61 CNV\_WT\_CLKN <<<<—

61 CNV\_WR\_DP1 >>>>—  
61 CNV\_WR\_DN1 >>>>—  
61 CNV\_WR\_DP0 >>>>—  
61 CNV\_WR\_DN0 >>>>—  
61 CNV\_WR\_CLKP >>>>—  
61 CNV\_WR\_CLKN >>>>—

## WWAN

62 WWAN\_CLK\_CPU\_P <<<<—  
62 WWAN\_CLK\_CPU\_N <<<<—

## CARD

33 CARD\_CLK\_CPU\_N <<<<—  
33 CARD\_CLK\_CPU\_P <<<<—

6 CPU\_WAKE >>>>—

99 PCH\_JTAG\_TRST\_N <<<<—

20191023\_Ricky  
6 CPU\_PWRGD <<<<—

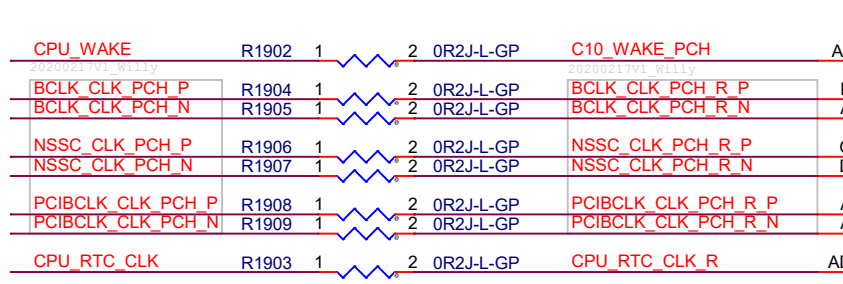
20200218V1\_Willy  
6 BCLK\_CLK\_PCH\_P <<<<—  
6 BCLK\_CLK\_PCH\_N <<<<—

6 NSSC\_CLK\_PCH\_P <<<<—  
6 NSSC\_CLK\_PCH\_N <<<<—

6 PCIBCLK\_CLK\_PCH\_P <<<<—  
6 PCIBCLK\_CLK\_PCH\_N <<<<—

6 CPU\_RTC\_CLK <<<<—

<https://vinafix.com>



20191023\_Ricky

CNV\_WT\_DP1 AU16  
CNV\_WT\_DN1 AW15

CNV\_WT\_DP0 AY15  
CNV\_WT\_DN0 BA14

CNV\_WT\_CLKP AU14  
CNV\_WT\_CLKN AW13

CNV\_WR\_DP1 BE11  
CNV\_WR\_DN1 BD11

CNV\_WR\_DP0 BD13  
CNV\_WR\_DN0 BC13

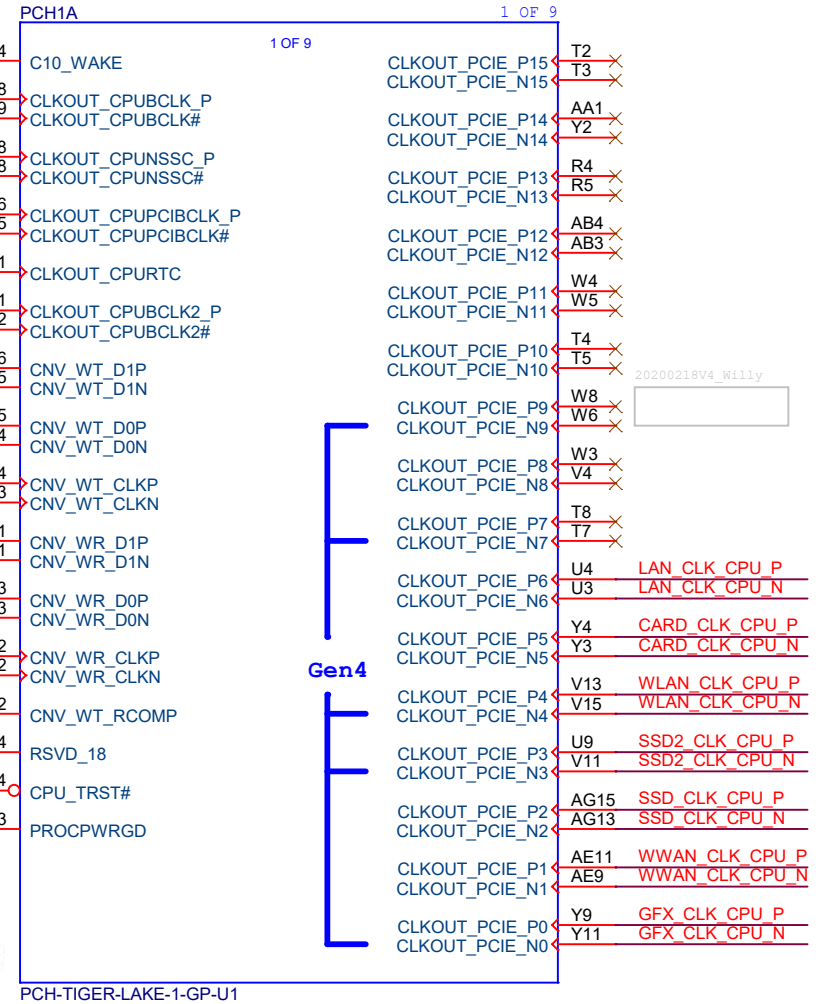
CNV\_WR\_CLKP BD12  
CNV\_WR\_CLKN BC12

R1901 2 150R2F-1-GP CNV\_WT\_RCOMP BE12

20200218V5\_Willy

PCH\_JTAG\_TRST\_N AE4

CPU\_PWRGD AC3



20200218V4\_Willy

Gen4

CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	0	Yes	<b>PCI Express* Clock Output:</b> PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices. <ul style="list-style-type: none"><li>CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support</li><li>CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support</li></ul>
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<Variant Name>

緯創資通

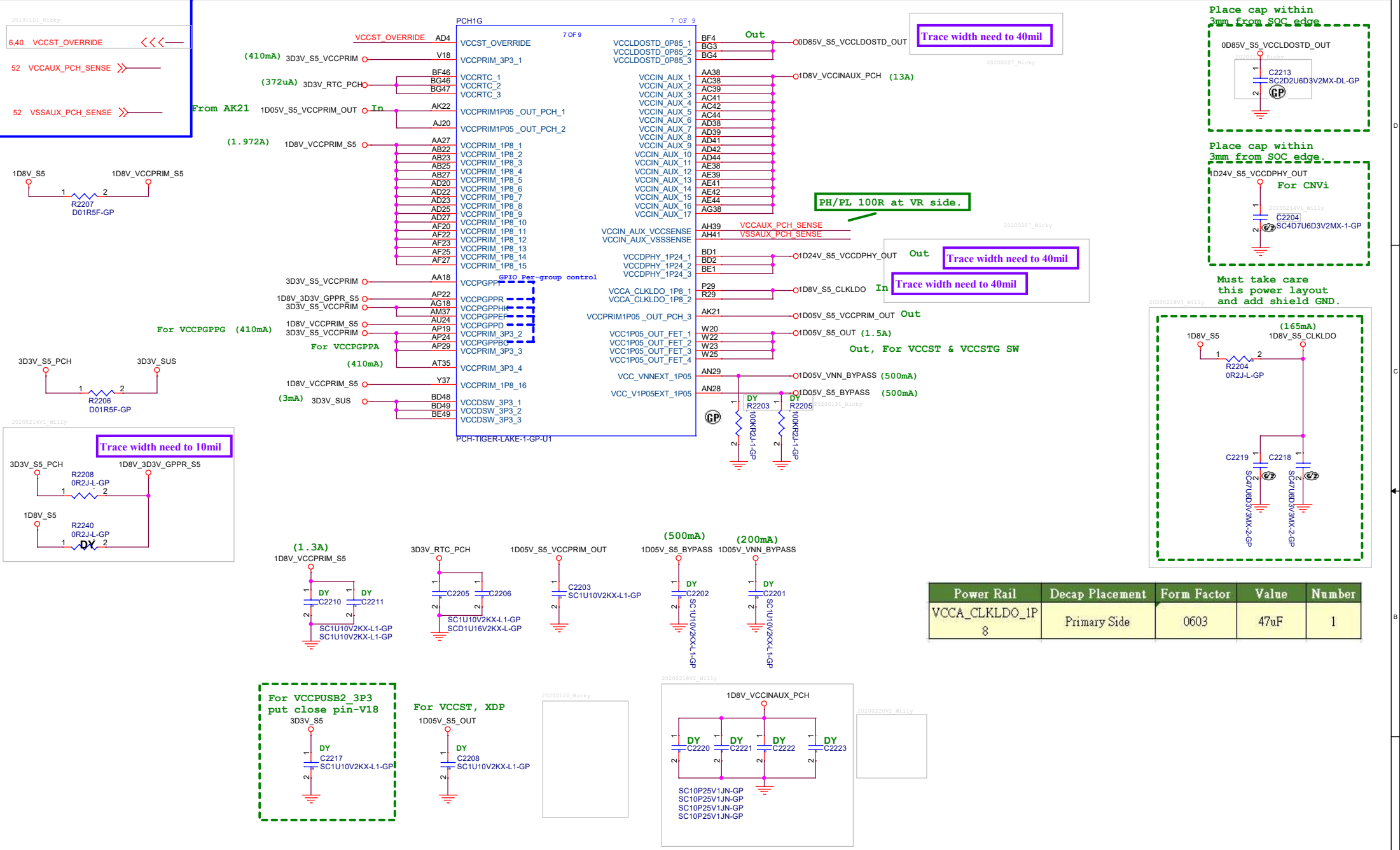
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>019_PCH (CLK/CNVi)</b>		
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>	Rev <b>X01</b>
Date Monday, October 26, 2020	Sheet 19	of 106







Power Rail	Decap Placement	Form Factor	Value	Number
VCCA_CLKLDO_1P8	Primary Side	0603	47uF	1

PCH1H 8 OF 9			PCH1H 8 OF 9		
A17	VSS_163	VSS_240	AJ23		
A2	VSS_164	VSS_241	AJ25		
A28	VSS_165	VSS_242	AJ27		
A3	VSS_166	VSS_243	AJ28		
A33	VSS_167	VSS_244	AK12		
A37	VSS_168	VSS_245	AK17		
A4	VSS_169	VSS_246	AK18		
A41	VSS_170	VSS_247	AK24		
A45	VSS_171	VSS_248	AK25		
A46	VSS_172	VSS_249	AK26		
A47	VSS_173	VSS_250	AK28		
A48	VSS_174	VSS_251	AK29		
AA12	VSS_175	VSS_252	AK30		
AA13	VSS_176	VSS_253	AK32		
AA20	VSS_177	VSS_254	AK33		
AA22	VSS_178	VSS_255	AK35		
AA23	VSS_179	VSS_256	AK38		
AA25	VSS_180	VSS_257	AK45		
AA29	VSS_181	VSS_258	AK5		
AA30	VSS_182	VSS_259	AL19		
AA32	VSS_183	VSS_260	AL22		
AA33	VSS_184	VSS_261	AL24		
AA35	VSS_185	VSS_262	AL25		
AA37	VSS_186	VSS_263	AL26		
AA49	VSS_187	VSS_264	AL28		
AA5	VSS_188	VSS_265	AL29		
AB28	VSS_189	VSS_266	AL31		
AC13	VSS_190	VSS_267	AM1		
AC18	VSS_191	VSS_268	AM12		
AC35	VSS_192	VSS_269	AM17		
AC37	VSS_193	VSS_270	AM33		
AC4	VSS_194	VSS_271	AM35		
AC45	VSS_195	VSS_272	AM38		
AC5	VSS_196	VSS_273	AM49		
AC9	VSS_197	VSS_274	AN17		
AD11	VSS_198	VSS_275	AN19		
AD12	VSS_199	VSS_276	AN22		
AD13	VSS_200	VSS_277	AN24		
AD15	VSS_201	VSS_278	AN25		
AD17	VSS_202	VSS_279	AN26		
AD18	VSS_203	VSS_280	AN31		
AD28	VSS_204	VSS_281	AN33		
AD35	VSS_205	VSS_282	AP12		
AD37	VSS_206	VSS_283	AP17		
AD45	VSS_207	VSS_284	AP21		
AD49	VSS_208	VSS_285	AP25		
AD5	VSS_209	VSS_286	AP26		
AD6	VSS_210	VSS_287	AP28		
AD8	VSS_211	VSS_288	AP31		
AD9	VSS_212	VSS_289	AP33		
AE12	VSS_213	VSS_290	AP38		
AE13	VSS_214	VSS_291	AP45		
AE15	VSS_215	VSS_292	AP5		
AE17	VSS_216	VSS_293	AT1		
AE18	VSS_217	VSS_294	AT12		
AE35	VSS_218	VSS_295	AT17		
AE37	VSS_219	VSS_296	AT19		
AE45	VSS_220	VSS_297	AT21		
AE5	VSS_221	VSS_298	AT22		
AF28	VSS_222	VSS_299	AT24		
AG1	VSS_223	VSS_300	AT25		
AG12	VSS_224	VSS_301	AT26		
AG17	VSS_225	VSS_302	AT28		
AG20	VSS_226	VSS_303	AT29		
AG22	VSS_227	VSS_304	AT31		
AG23	VSS_228	VSS_305	AT33		
AG25	VSS_229	VSS_306	AT37		
AG27	VSS_230	VSS_307	AT49		
AG28	VSS_231	VSS_308	AT5		
AG35	VSS_232	VSS_309	AU25		
AG37	VSS_233	VSS_310	AU41		
AG49	VSS_234	VSS_311	AV11		
AH12	VSS_235	VSS_312	AV39		
AH13	VSS_236	VSS_313	AV45		
AH15	VSS_237	VSS_314	AV5		
AH35	VSS_238	VSS_315	AW11		
AH38	VSS_239	VSS_316	AW24		



PCH-TIGER-LAKE-1-GP-U1

PCH1I 9 OF 9			PCH1I 9 OF 9		
AW25	VSS_1	VSS_78	F42		
AW39	VSS_2	VSS_79	F8		
AY25	VSS_3	VSS_80	G1		
AY43	VSS_4	VSS_81	G41		
AY5	VSS_5	VSS_82	G48		
AY7	VSS_6	VSS_83	G49		
B1	VSS_7	VSS_84	G9		
B2	VSS_8	VSS_85	H25		
B4	VSS_9	VSS_86	H43		
B46	VSS_10	VSS_87	H8		
B48	VSS_11	VSS_88	J11		
B49	VSS_12	VSS_89	J25		
B6	VSS_13	VSS_90	J39		
BA41	VSS_14	VSS_91	J9		
BA43	VSS_15	VSS_92	K11		
BA49	VSS_16	VSS_93	K39		
BA9	VSS_17	VSS_94	K45		
BB25	VSS_18	VSS_95	K5		
BB44	VSS_19	VSS_96	L14		
BB8	VSS_20	VSS_97	L25		
BC11	VSS_21	VSS_98	M12		
BC15	VSS_22	VSS_99	M17		
BC19	VSS_23	VSS_100	M19		
BC24	VSS_24	VSS_101	M21		
BC25	VSS_25	VSS_102	M22		
BC26	VSS_26	VSS_103	M24		
BC31	VSS_27	VSS_104	M25		
BC35	VSS_28	VSS_105	M26		
BC39	VSS_29	VSS_106	M28		
BC41	VSS_30	VSS_107	M29		
BC9	VSS_31	VSS_108	M31		
BF1	VSS_32	VSS_109	M33		
BF13	VSS_33	VSS_110	M38		
BF2	VSS_34	VSS_111	M49		
BF42	VSS_35	VSS_112	M5		
BF48	VSS_36	VSS_113	P12		
BF49	VSS_37	VSS_114	P21		
BG17	VSS_38	VSS_115	P24		
BG2	VSS_39	VSS_116	P25		
BG22	VSS_40	VSS_117	P28		
BG25	VSS_41	VSS_118	P38		
BG28	VSS_42	VSS_119	P4		
BG33	VSS_43	VSS_120	P45		
BG37	VSS_44	VSS_121	R21		
BG41	VSS_45	VSS_122	R24		
BG48	VSS_46	VSS_123	R25		
BG9	VSS_47	VSS_124	R28		
C1	VSS_48	VSS_125	T1		
C12	VSS_49	VSS_126	T12		
C24	VSS_50	VSS_127	T15		
C4	VSS_51	VSS_128	T17		
C49	VSS_52	VSS_129	T33		
C7	VSS_53	VSS_130	T38		
D1	VSS_54	VSS_131	T49		
D13	VSS_55	VSS_132	U19		
D2	VSS_56	VSS_133	U21		
D24	VSS_57	VSS_134	U22		
D25	VSS_58	VSS_135	U24		
D33	VSS_59	VSS_136	U25		
D37	VSS_60	VSS_137	U26		
D48	VSS_61	VSS_138	U28		
D49	VSS_62	VSS_139	U29		
D7	VSS_63	VSS_140	U31		
E13	VSS_64	VSS_141	V12		
E15	VSS_65	VSS_142	V17		
E19	VSS_66	VSS_143	V21		
E22	VSS_67	VSS_144	V22		
E24	VSS_68	VSS_145	V24		
E25	VSS_69	VSS_146	V25		
E28	VSS_70	VSS_147	V26		
E31	VSS_71	VSS_148	V33		
E33	VSS_72	VSS_149	V38		
E35	VSS_73	VSS_150	V5		
E37	VSS_74	VSS_151	W27		
E39	VSS_75	VSS_152	W28		
E9	VSS_76	VSS_153	W30		
F25	VSS_77	VSS_154	W44		
	VSS_155	VSS_156	Y12		
	VSS_157	VSS_158	Y13		
	VSS_159	VSS_160	Y15		
	VSS_161	VSS_162	Y17		
			Y18		
			Y32		
			Y38		



PCH-TIGER-LAKE-1-GP-U1

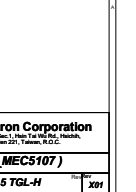
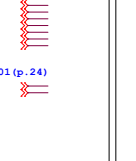
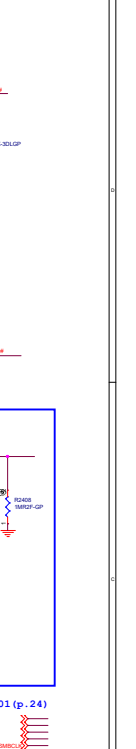
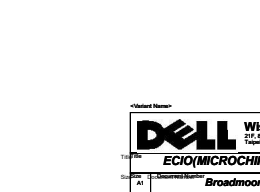
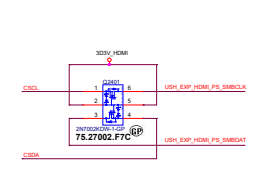
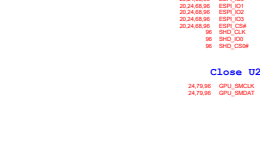
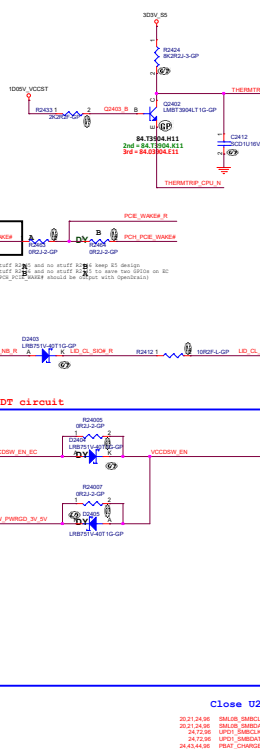
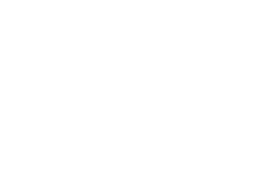
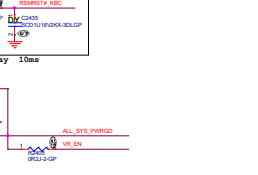
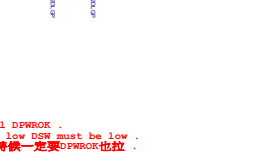
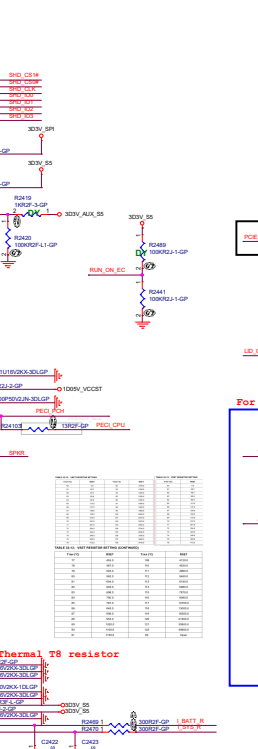
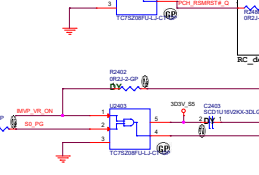
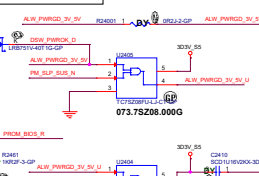
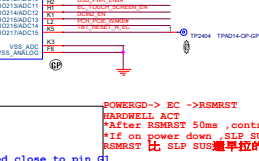
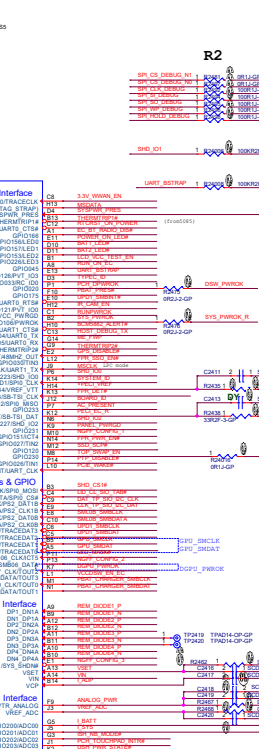
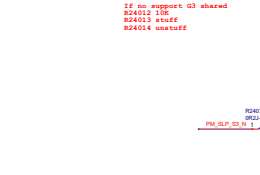
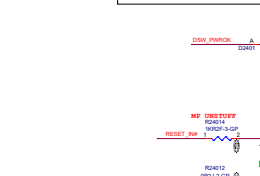
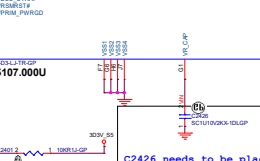
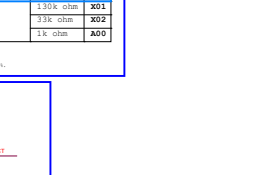
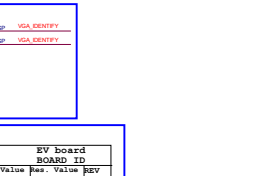
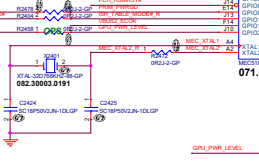
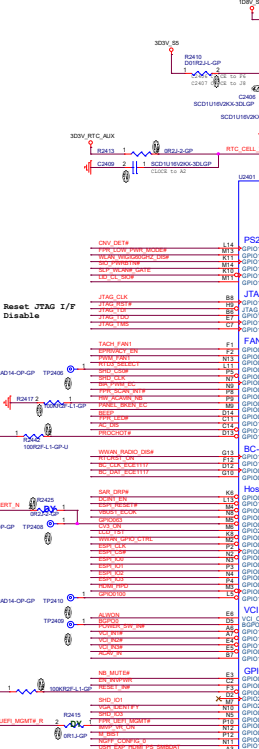
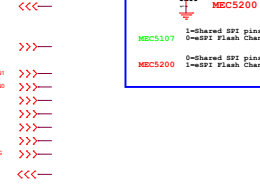
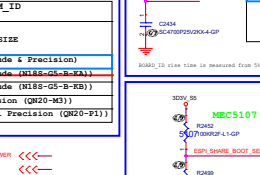
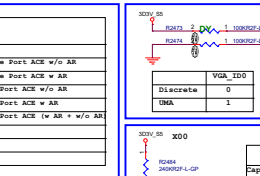
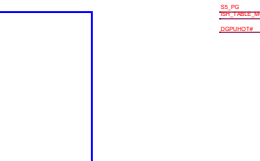
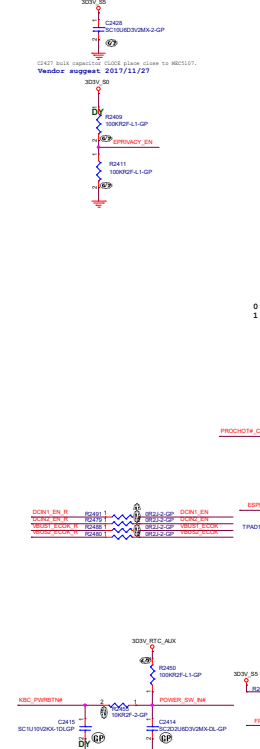
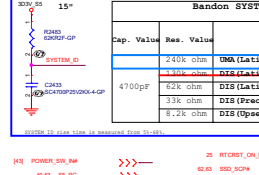
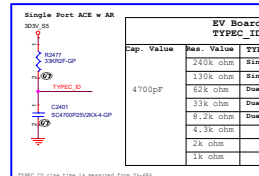
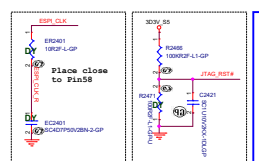
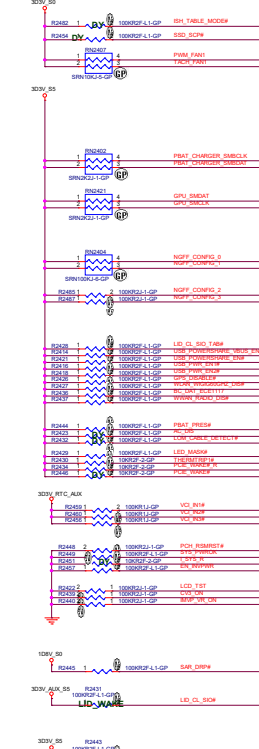
<Variant Name>

 <b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		
<b>Title</b> 023_PCH (VSS)		
<b>Size</b> A3	<b>Document Number</b> Broadmoor 15 TGL-H	<b>Rev</b> X01
<b>Date:</b> Monday, October 26, 2020		
Sheet 23 of 106		



Main Func = EC

- 61 WLAN\_WAKEUP\_DSX
- 62 WLAN\_WAKEUP\_DSX
- 63 WLAN\_WAKEUP\_DSX
- 64 WLAN\_WAKEUP\_DSX
- 65 WLAN\_WAKEUP\_DSX
- 66 WLAN\_WAKEUP\_DSX
- 67 WLAN\_WAKEUP\_DSX
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- 194 WLAN\_WAKEUP\_DSX
- 195 WLAN\_WAKEUP\_DSX
- 196 WLAN\_WAKEUP\_DSX
- 197 WLAN\_WAKEUP\_DSX
- 198 WLAN\_WAKEUP\_DSX
- 199 WLAN\_WAKEUP\_DSX
- 200 WLAN\_WAKEUP\_DSX



https://vinafix.com

## Main Func = BIOS ROM/RTC

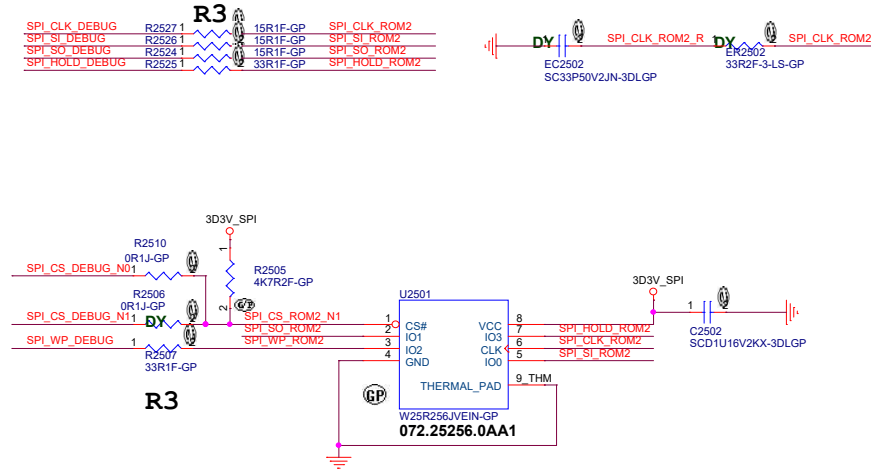
## SYSTEM SPI ROM

24.68.91 SPI\_CLK\_DEBUG >>>  
24.68.91 SPI\_SI\_DEBUG >>>  
24.68.91 SPI\_SO\_DEBUG >>>  
24.68 SPI\_WP\_DEBUG >>>  
24.68 SPI\_HOLD\_DEBUG >>>  
24.68 SPI\_CS\_DEBUG\_N0 >>>  
24.68 SPI\_CS\_DEBUG\_N1 >>>

24 VCCDSW\_EN\_EC >>>  
24 RTCRST\_ON\_POWER >>>  
20 RTC\_DET#\_1P8 <<<

Close U2501(p.25)

96 SPI\_CLK\_ROM2 >>>  
96 SPI\_SI\_ROM2 >>>  
96 SPI\_CS\_ROM2\_N1 >>>

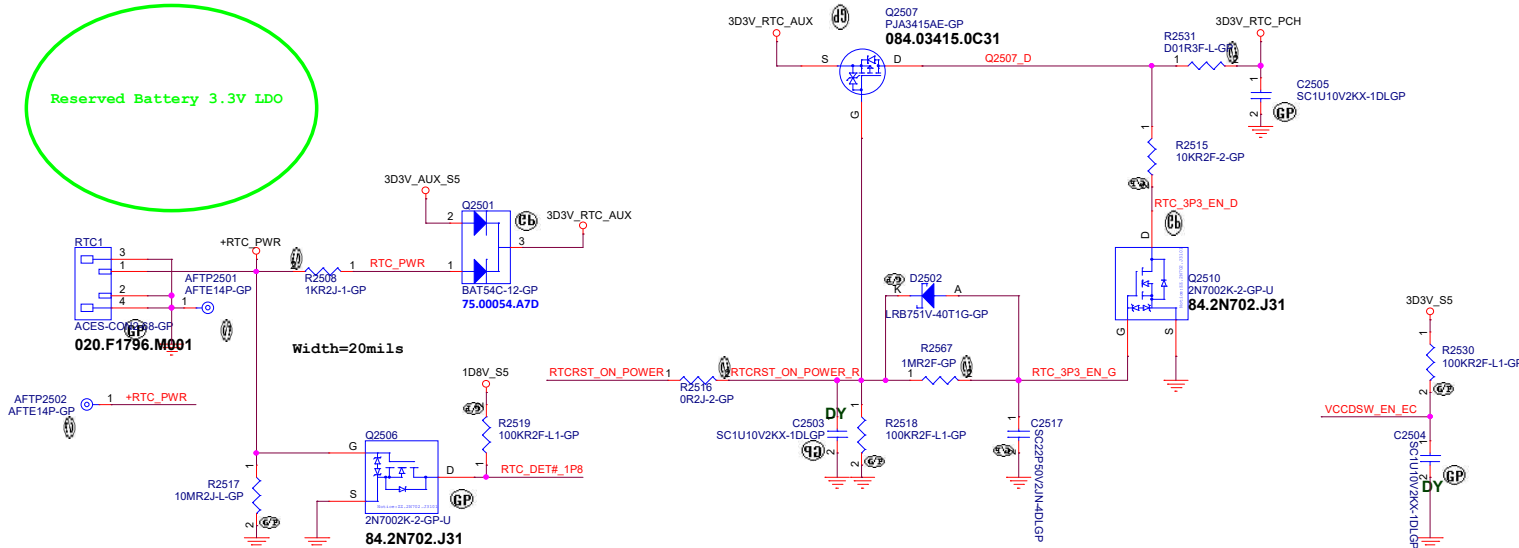


Non-vPRO configs - 16MB (UI)  
Winbond W25Q128JVS1Q; MXIC: MX25L12873FM; GigaDevice: GD25B127D  
If more than 3 sources are required then these parts can be considered:  
Spansion: S25FL128L; Micron: MT25QL128ABA1ESE-0S1T

vPRO Configs: 32MB  
Winbond W25Q256JV, GigaDevice GD25Q256C, Cypress S25FL256L

WinBond	WSON (8x6)		8-pin SOP (208mil)	
	Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
ROM size				
8M Byte	072.25Q64.0B03	W25Q64JVE1Q	072.25Q64.0B01	W25Q64JVS1Q
16 M Byte	072.25128.0A11	W25Q128JVE1Q	072.25128.0B51	W25Q128JVS1Q
32 M Byte	072.25256.0N01	W25Q256JVE1Q		N/A
MXIC	WSON (8x6)		8-pin SOP (208mil)	
	Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
ROM size				
8M Byte	072.25643.0B01	MX25L643972J	072.25643.0B01	MX25L643972J-080
16 M Byte	XX	XX	072.25673.0B01	MX25L12873FM1-100
32 M Byte	072.25673.0B03	MX25L2567302-100	072.25673.0B01	MX25L2567302-080
GIGADEVICE	WSON (8x6)		SOP8 208MIL	
	Wistron Part No.	Vendor Part No.	Wistron Part No.	Vendor Part No.
ROM size				
8M Byte	072.02564.0B01	GD25B64C1GR	072.25643.0B01	GD25B64C1GR
16 M Byte			072.25127.0B01	GD25B127DS1GR
32 M Byte	072.25256.0B03	GD25B256Y1GR		

## X09 design DS3\_Non-DS3 with RTC power gating



&lt;Variant Name&gt;

DELL		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Flash/RTC			
Size	Document Number	Broadmoor 15 TGL-H	
Custom		X01	
Date	Monday, October 26, 2020	Sheet	25 of 106



24 REM\_DIODE4\_P  
24 REM\_DIODE4\_N  
24 PWM\_FAN1  
24 TACH\_FAN1

3D3V\_S0

U2601

PWM\_FAN1 1 6 PWM\_FAN1\_Q

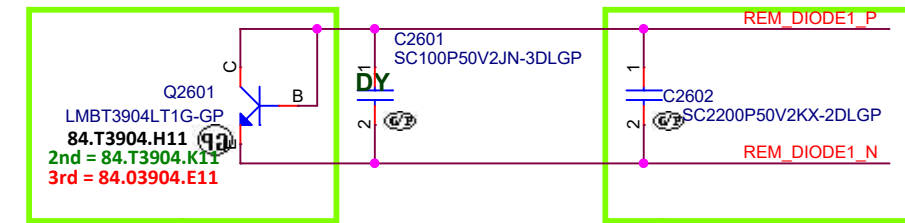
2 5

TACH\_FAN1\_Q 3 4 TACH\_FAN1

2N7002KDW-1-GP

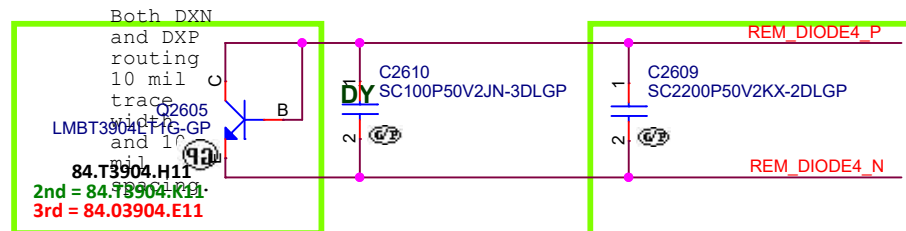
75.27002.F7C

GP

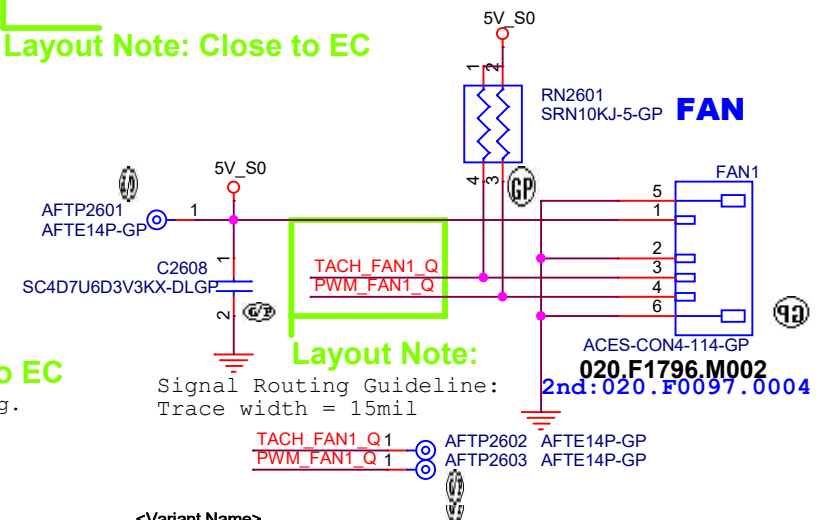


Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

**Layout Note: Close to EC**



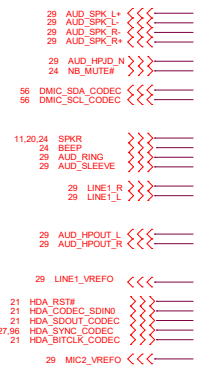
Both DXN and DXP routing 10 mil trace width and 10 mil spacing.



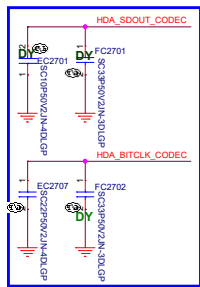
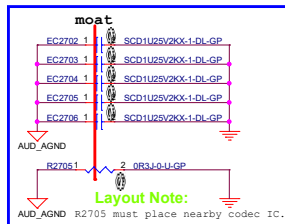
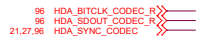
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Date:	Monday, October 26, 2020	Sheet	26	of	106
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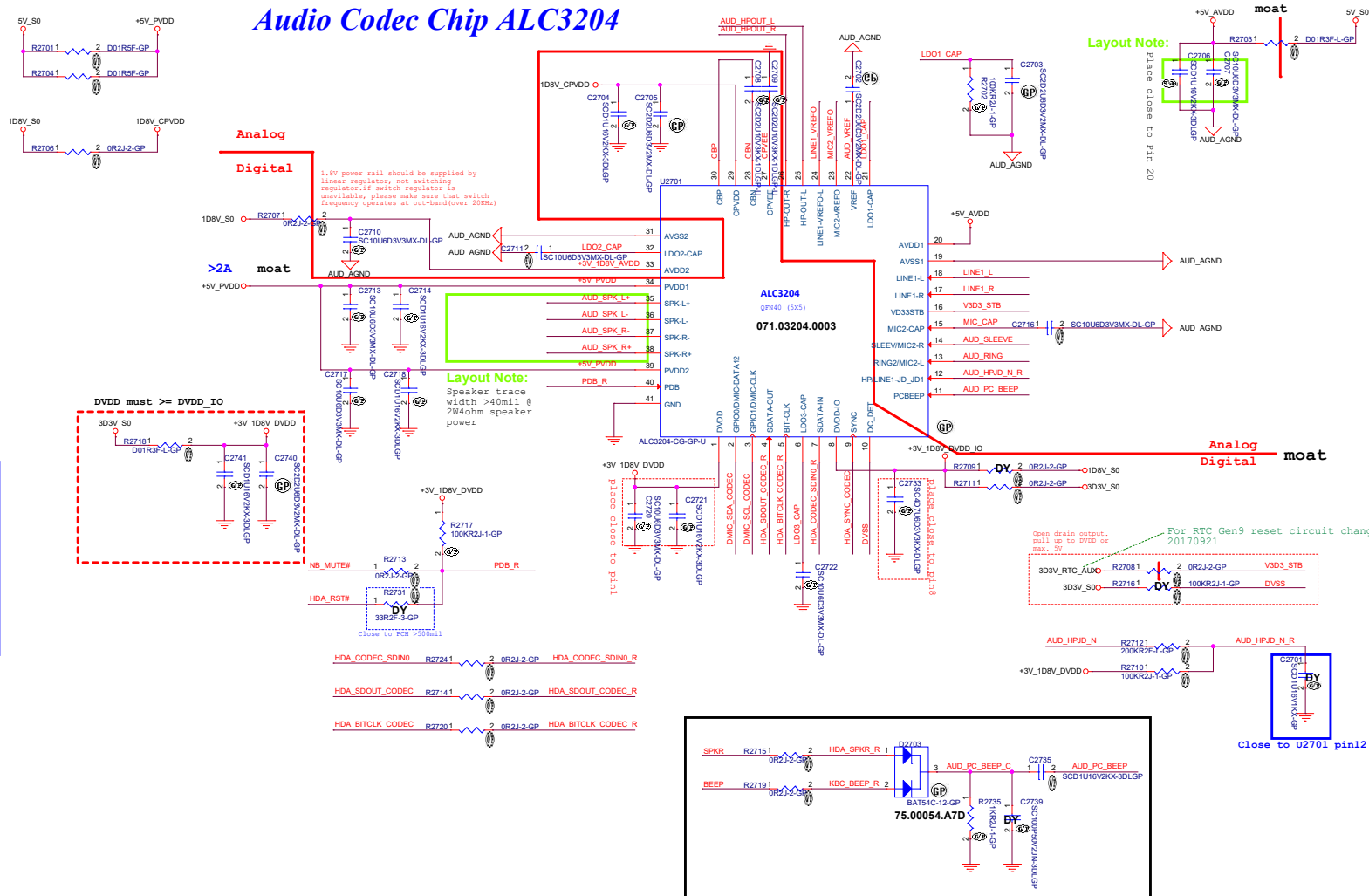
Main Func = Audio



Close U2701 (p.27)




## Audio Codec Chip ALC3204



5	4	3	2	1
D				
C				
B				
A				

<https://vinafix.com>

<Variant Name>

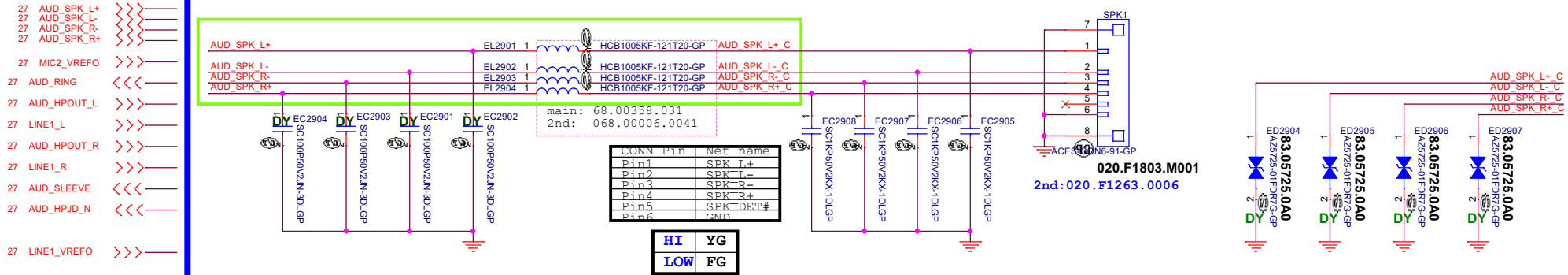
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Audio (RSVD) (Audio AMP)</b>		
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 28 of 106

# Main Func = Audio

## Layout Note:

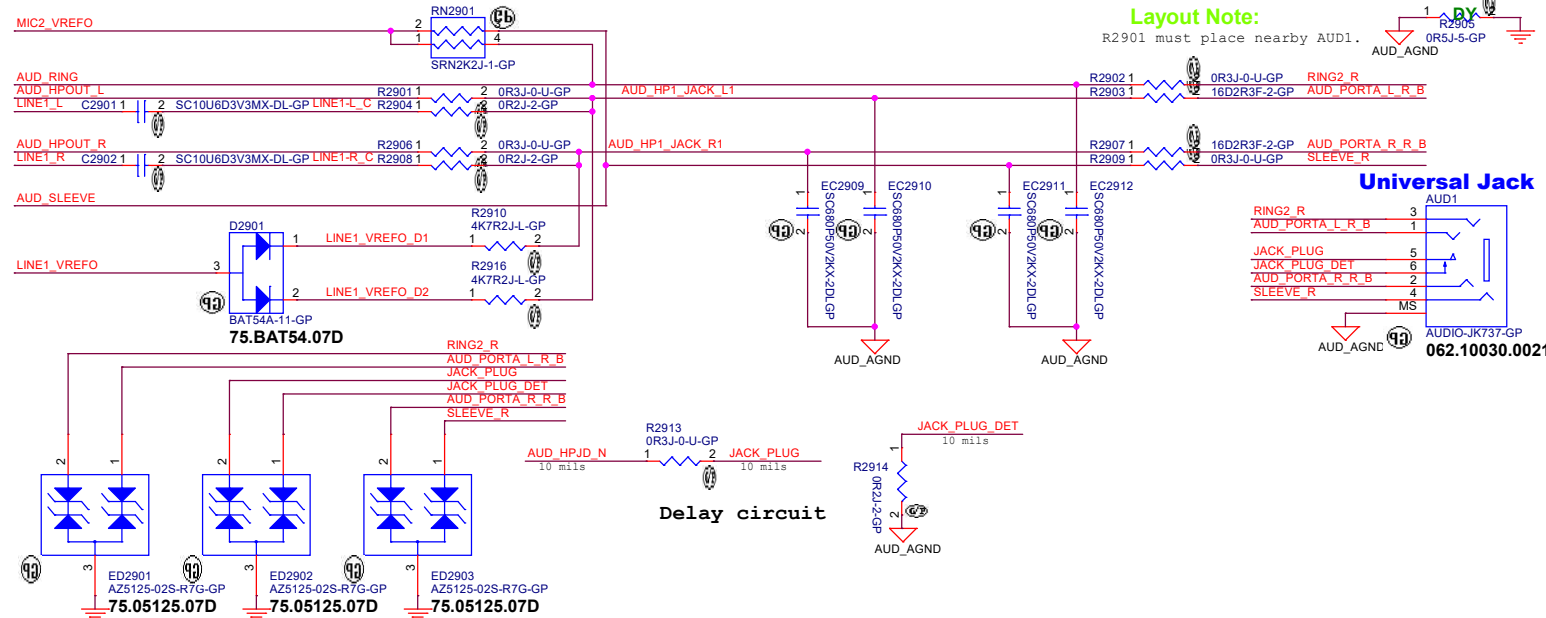
Speaker trace width >40mil @ 2W4ohm speaker power

## Speaker



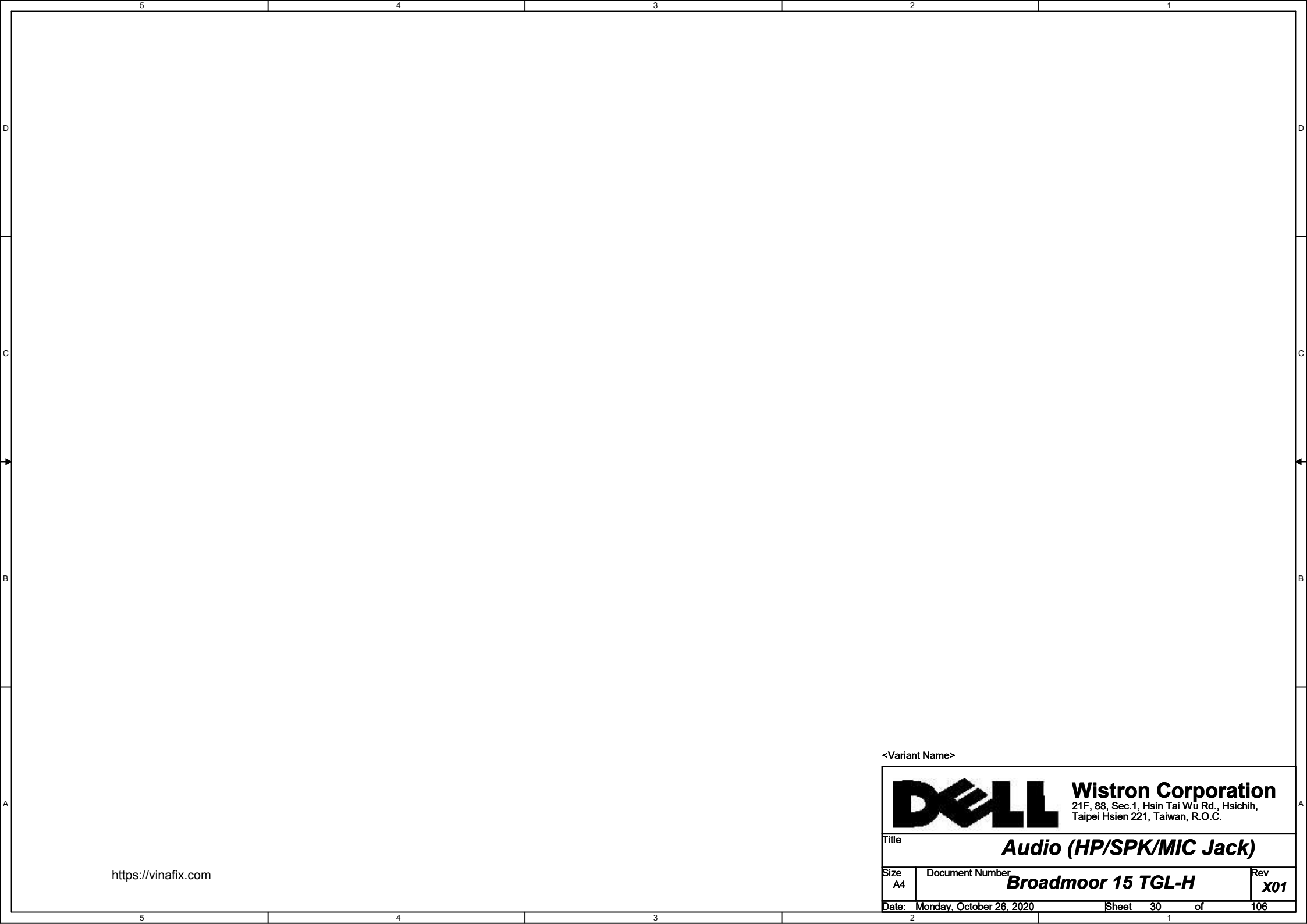
## Layout Note:

R2901 must place nearby AUD1.




<Variant Name>

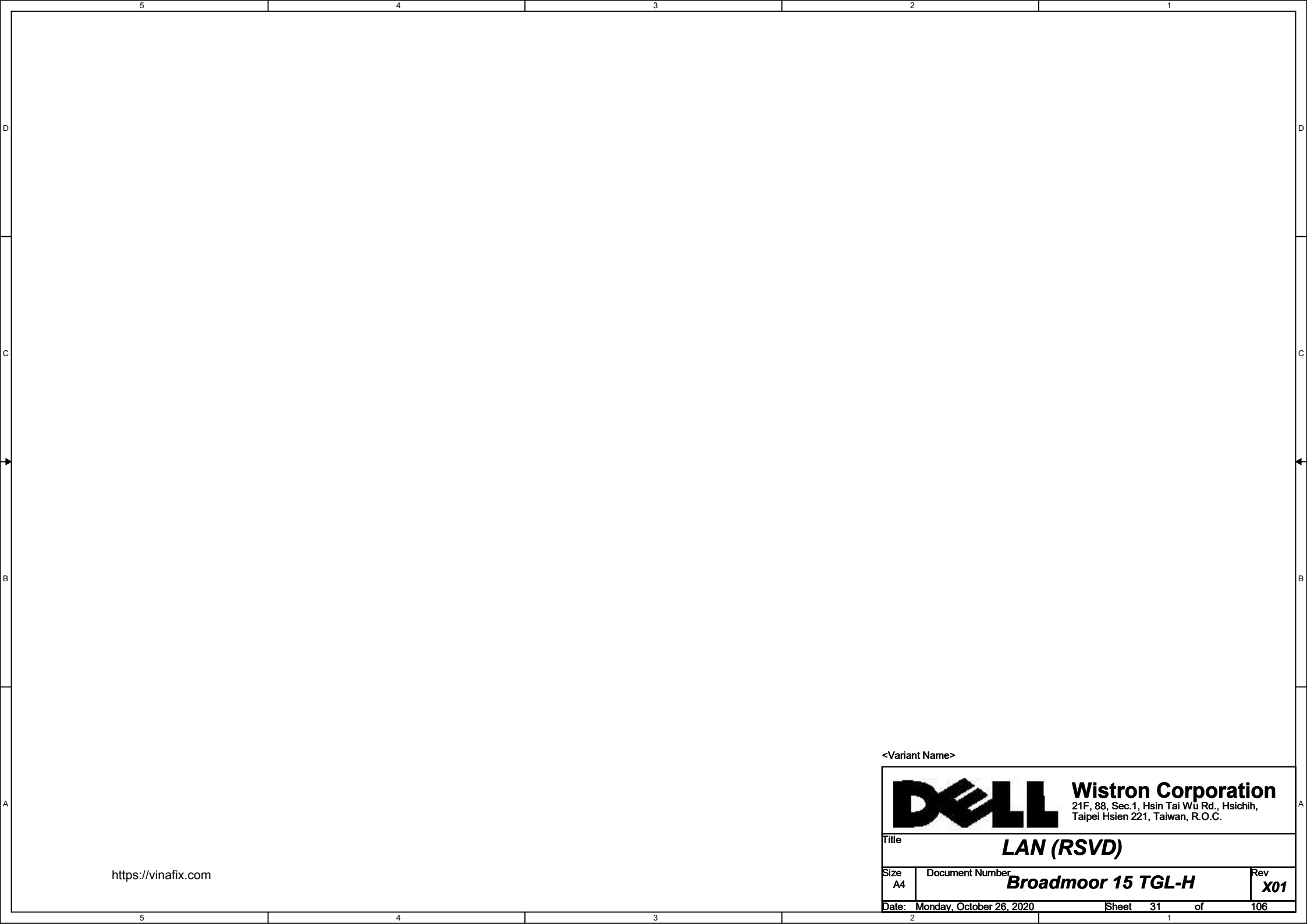
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
<b>Audio (HP/SPK/MIC Jack)</b>		
Size A3	Document Number	Rev X01
Date: Monday, October 26, 2020		Sheet 29 of 106



<https://vinafix.com>


<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Audio (HP/SPK/MIC Jack)</b>		
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 30 of 106



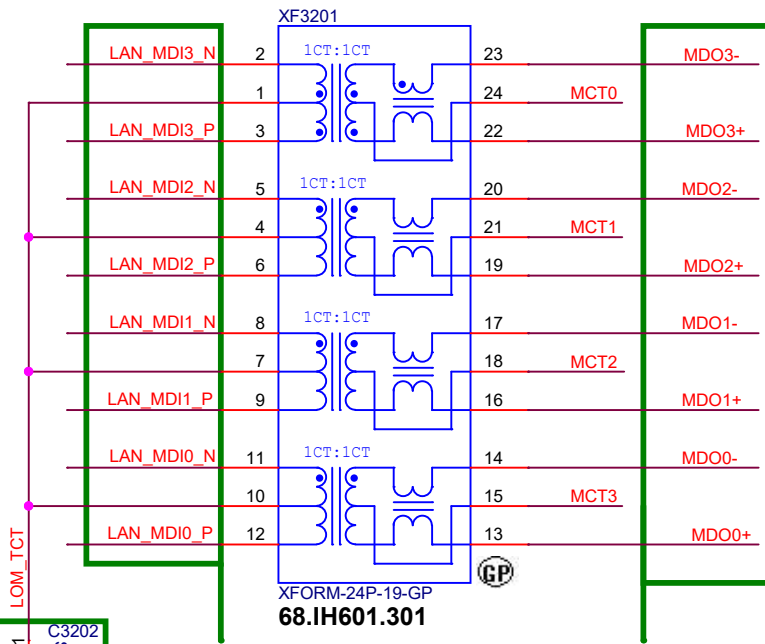
<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LAN (RSVD)</b>			
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>		Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 31 of	106

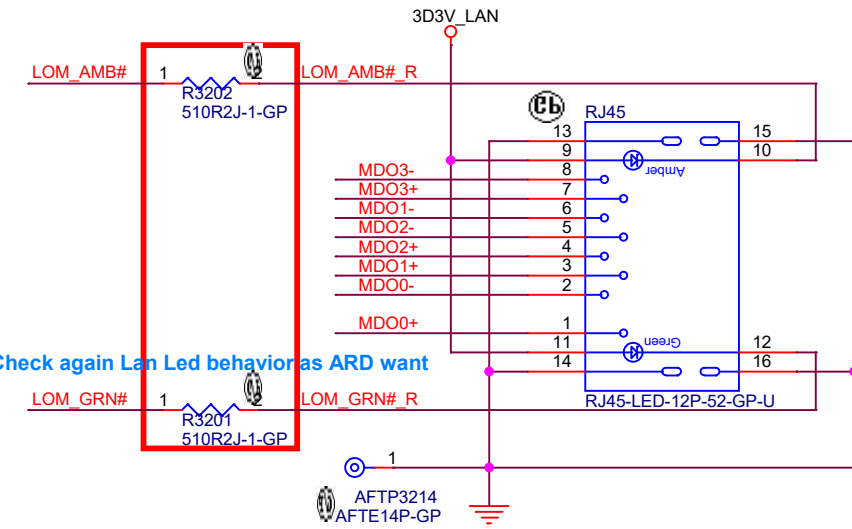
# Main Func = LAN

24,64 LED\_MASK#  
 97 LAN\_0\_GREEN\_LINK\_N  
 97 LAN\_1\_AMBER\_ACT\_N  
 97 LAN\_MDI0\_P  
 97 LAN\_MDI0\_N  
 97 LAN\_MDI1\_P  
 97 LAN\_MDI1\_N  
 97 LAN\_MDI2\_P  
 97 LAN\_MDI2\_N  
 97 LAN\_MDI3\_P  
 97 LAN\_MDI3\_N

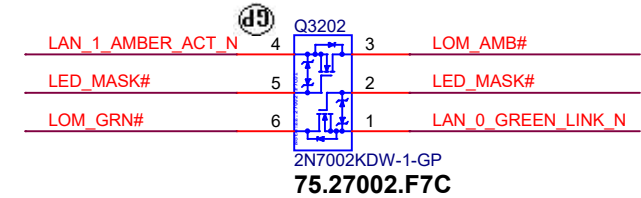


Layout note:  
 30 mil spacing between MDI differential pairs.

Follow Reference Schematic 0.01uF~0.4uF



Check again Lan Led behavior as ARD want



- LED0 (010): Green = Indicates Link connection established (located on left-hand side of connector)
- LED1 (011): Amber = Blinking when network activity (located on right-hand side of connector)

<Variant Name>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> LAN (RSVD) (RJ45+Transformer)			
<b>Size</b> A4	<b>Document Number</b> Broadmoor 15 TGL-H		<b>Rev</b> X01
<b>Date</b> Monday, October 26, 2020		<b>Sheet</b> 32	<b>of</b> 106

https://vinafix.com

3D3V S0 CARD

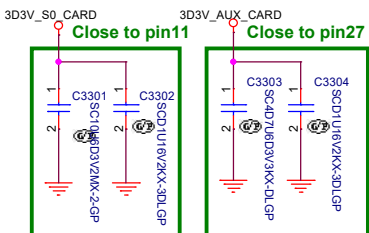
```

17 CARD_PCIE_RX_N    <<>>=====
17 CARD_PCIE_RX_P    <<>>=====
17 CARD_PCIE_TX_N    <<>>=====
17 CARD_PCIE_TX_P    <<>>=====

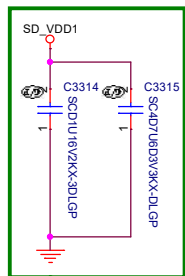
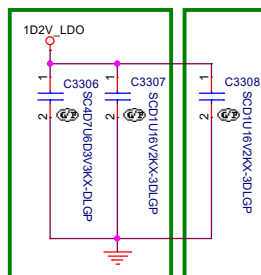
19 CARD_CLK_CPU_P     <<>>=====
19 CARD_CLK_CPU_N     <<>>=====
20 CARD_CLKREQ_CPU_N  <<>>=====
20 MEDIACARD_IRO#     <<>>=====

```

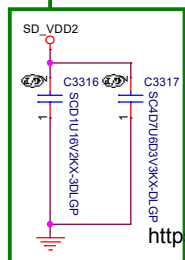
**Layout Note:**



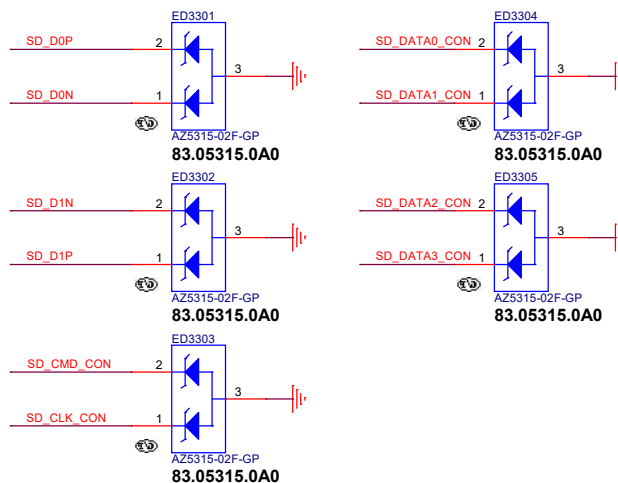
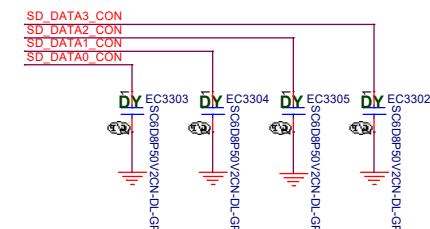
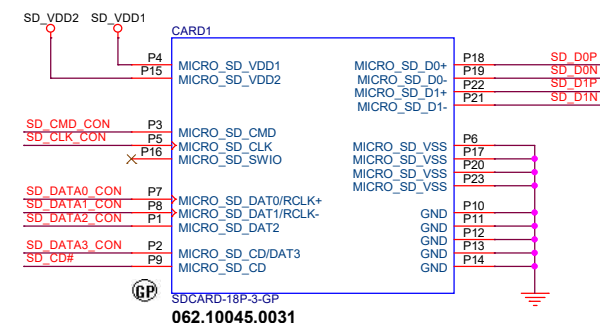
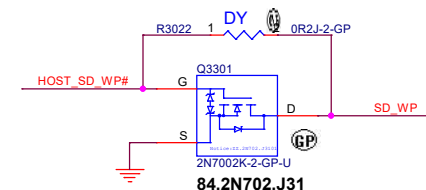
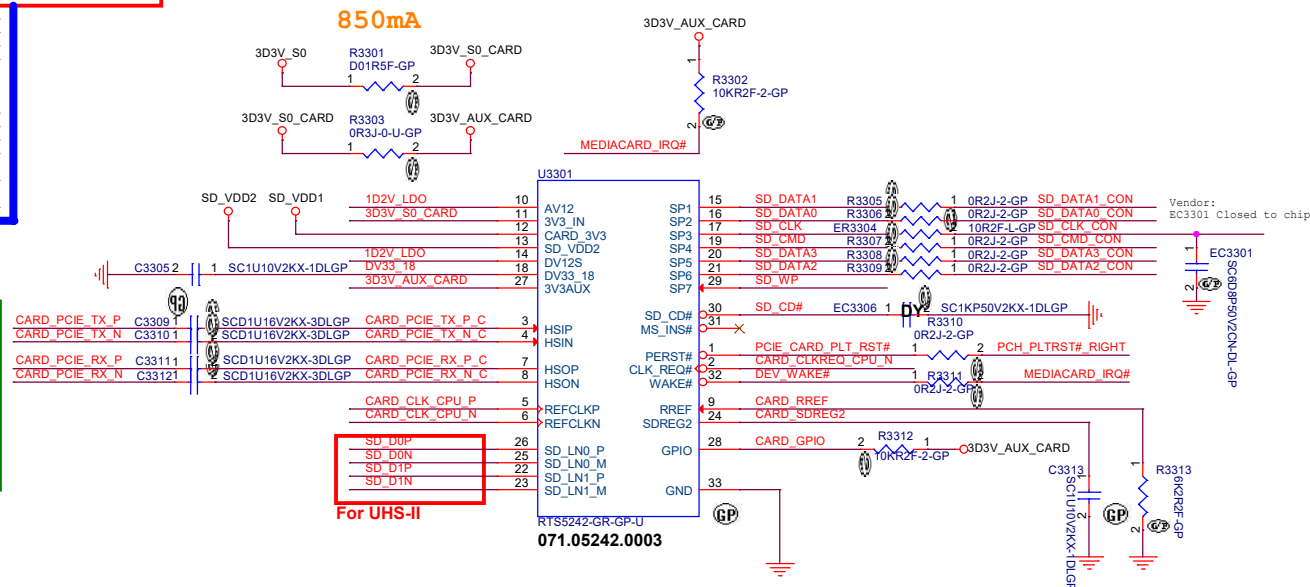
Close to pin14      Close to pin10



**Layout Note:Close to Card Reader CONN**



<https://vinafix.com>






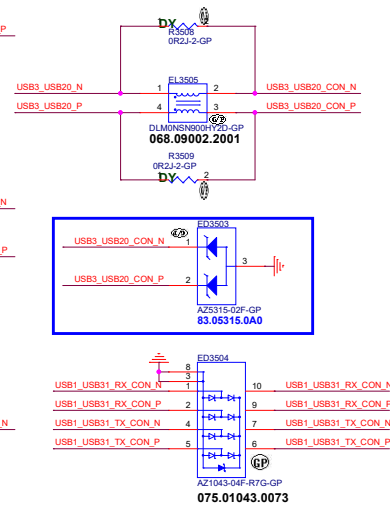
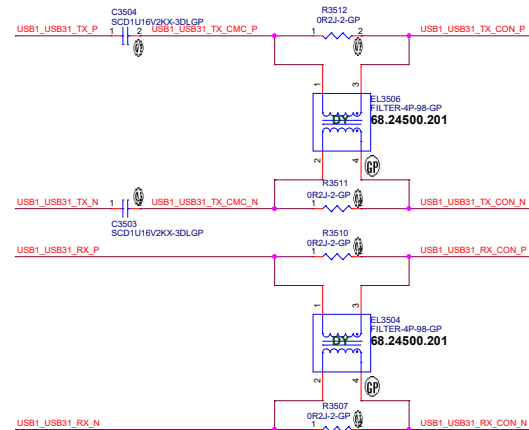
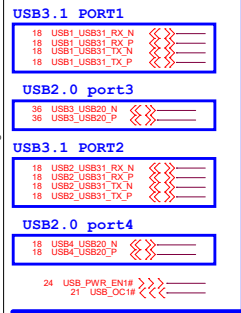
5	4	3	2	1
D				
C				
B				
A				

<https://vinafix.com>

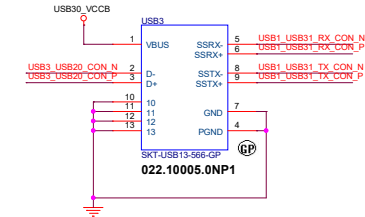
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>USB (RSVD) (USB2.0 CONN)</b>		
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 34 of 106

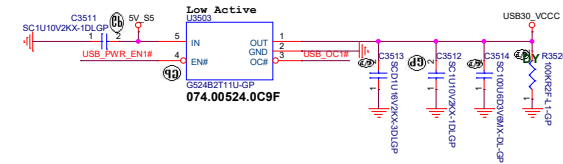
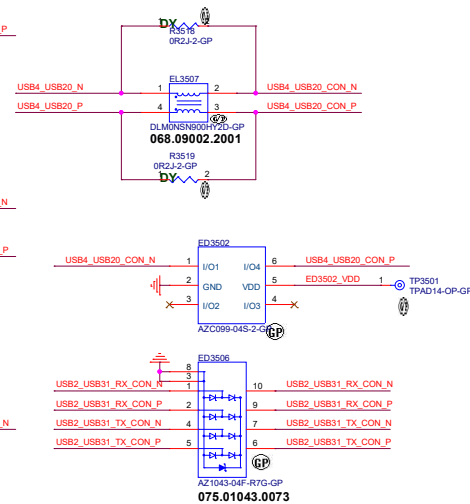
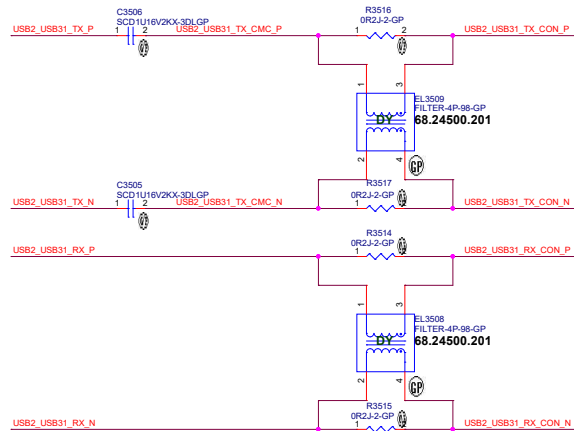
## USB3/USB32-1/USB20-3/PowerShare



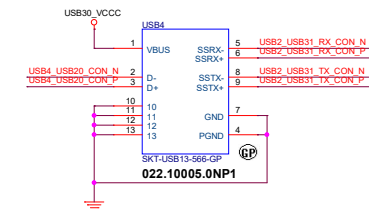
EXT Port1 Right Side, Support Power Share



USB4/USB32-2/USB20-4



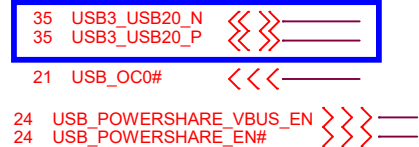
EXT Port1 Right Side, Support Power Share



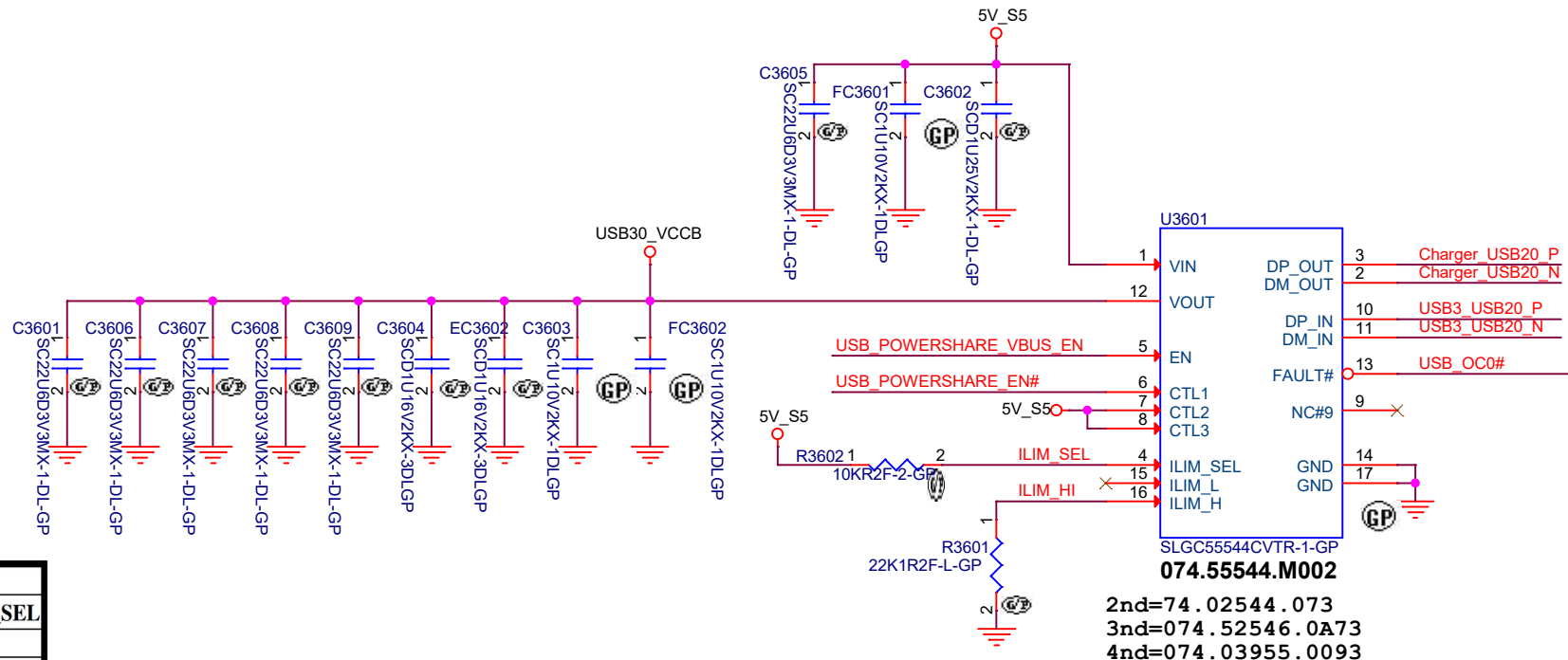
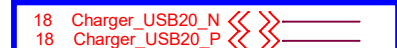
# Main Func = USB Charger

support power share on the USB3.0 port on the right side of platform

## USB2.0 port3



## USB charger



Device Control Pins

Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH(Discharge)	0	0	0	x
CDP	1	1	1	1
SDP2(No Discharge from/to CDP)	1	1	1	0
SDP1(Discharge from/to any charging state including CDP)	1	1	0	x
	0	1	0	x
DCP_Short	1	0	0	x
DCP/Divider-1A	1	0	1	x
DCP_Auto	0	1	1	x
	0	0	1	x

Current Limit	MIN	TPY	MAX
TI	2120	2275	2430
PERICOM	2120	2275	2430
NUVOTON	2235	2400	2570

<https://vinafix.com>

<Variant Name>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

**USB (USB Charger)**

Size  
A4

Document Number

**Broadmoor 15 TGL-H**

Rev  
X01

Date: Monday, October 26, 2020

Sheet 36 of 106

D

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**A**

<https://vinafix.com>

**<Variant Name>**



# Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

### ***USB (RSVD) (PCIE to USB3.0)***

Size  
A4

Document Number:

**Broadmoor 15 TGL-H**

Rev	X0
-----	----


Date: Monday, October 26, 2020

Sheet 37 of 106

5	4	3	2	1
D				
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<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>USB (RSVD) (USB Redriver/Hub)</b>		
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 38 of 106

5

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A

<https://vinafix.com>

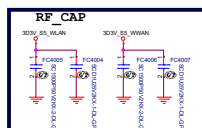
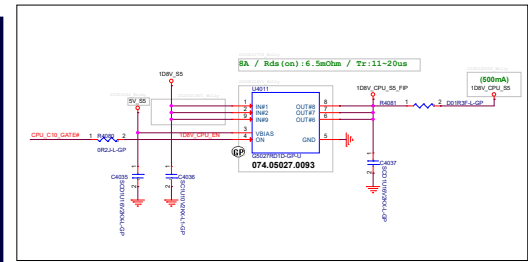
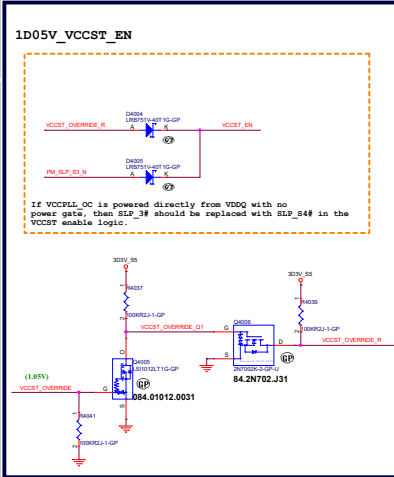
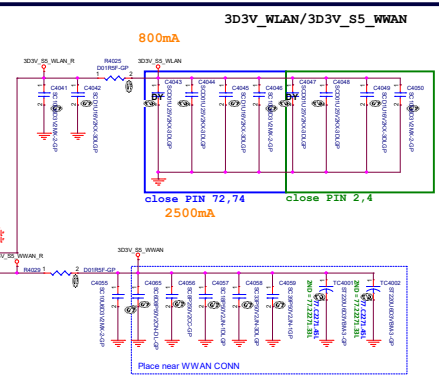
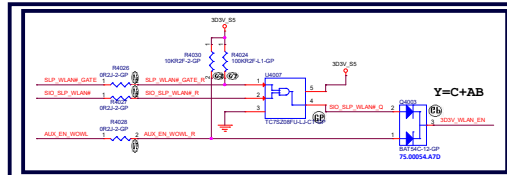
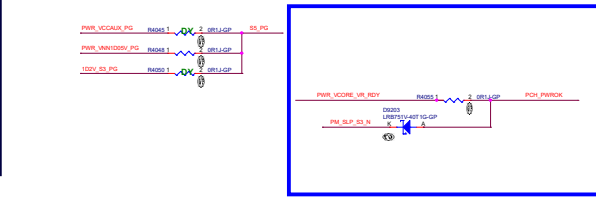
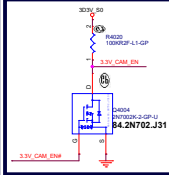
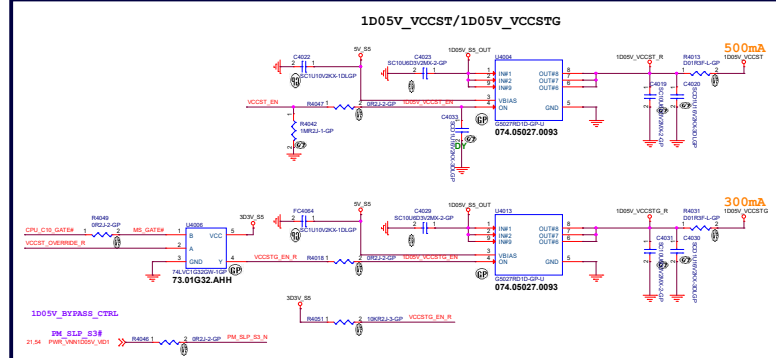
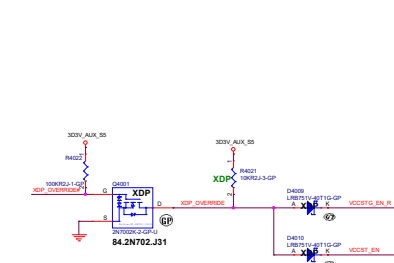
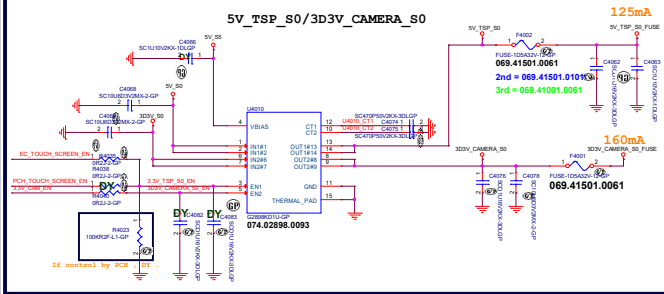
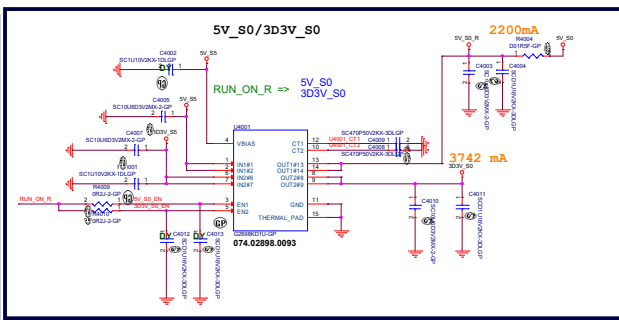
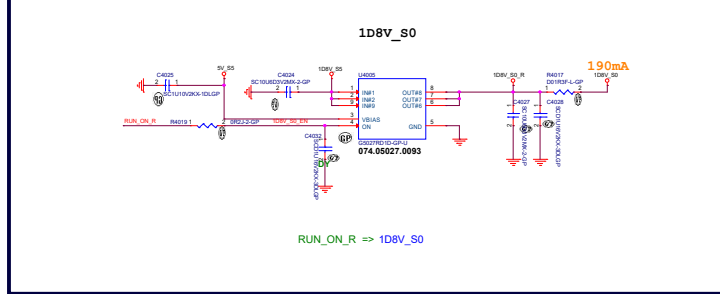
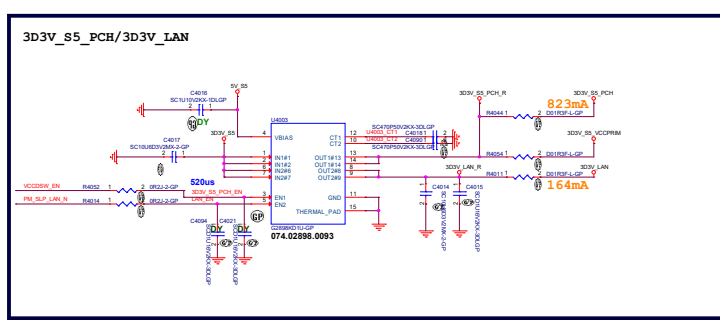
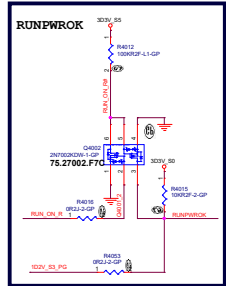
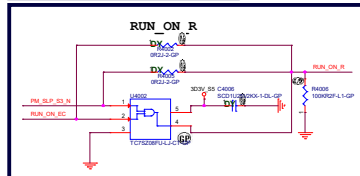
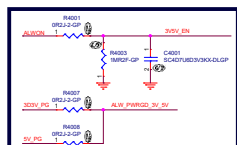
<Variant Name>

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<b>Sequence (RSVD)</b>					
Size		Document Number			Rev
A4		<b>Broadmoor 15 TGL-H</b>			<b>X01</b>
Date: Monday, October 26, 2020			Sheet 39 of 106		

Main Func = Power Plane EN Sequence

- 24.43 ALWON >>>
- 45 3V3V\_EN <<<
- 46 3V3V\_PG <<<
- 46 3V3V\_PG <<<
- 46 3V3V\_PG <<<
- 18 ALW\_PWRGD\_3V3V <<<
- 18 PM\_SLP\_LAN\_N <<<
- 24 SLP\_WLAN\_GATE <<<
- 18 SLP\_SLP\_WLAN <<<
- 18 ALW\_EN\_WWAN <<<
- 24 3V3V\_WWAN\_EN <<<
- 2191 CPU\_CLK\_GATEW >>>
- 77 RUN\_ON\_R >>>
- 2453 VCC3V3V\_EN >>>
- 10.2455 PM\_SLP\_S3\_N <<<
- 24 RUN\_ON\_EC <<<
- 24 RUNWPROK <<<
- 20 PCH\_TOUCH\_SCREEN\_EN <<<
- 20 PCH\_TOUCH\_SCREEN\_EN <<<
- 20 3V3V\_CAM\_ENW <<<
- 10.5185 PM\_SLP\_S3\_N <<<
- 51 100V\_S3\_PG <<<
- 10.53 PM\_SLP\_S3\_N <<<
- 50.52 PWR\_VCC3V3V\_PG <<<
- 54 PWR\_VCC3V3V\_PG <<<
- 54 PWR\_VCC3V3V\_PG <<<
- 6.22 VCC3V3V\_OVERIDE <<<
- 24.53 S3\_PG <<<
- 54 PWR\_VCC3V3V\_PG <<<
- 17.44 PCH\_PWRONK <<<
- PWR\_VCC3V3V\_PG <<<
- 50 VCC3V3V\_PG <<<

??? Not ready  
Should confirm with Dell






5	4	3	2	1
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<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Sequence (RSVD) (DS3/S0ix)</b>		
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 41 of 106

5

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<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>INT IO (RSVD)</b>			
Size A4	Document Number <b>Broadmoor 15 TGL-H</b>		Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 42 of	106

5

4

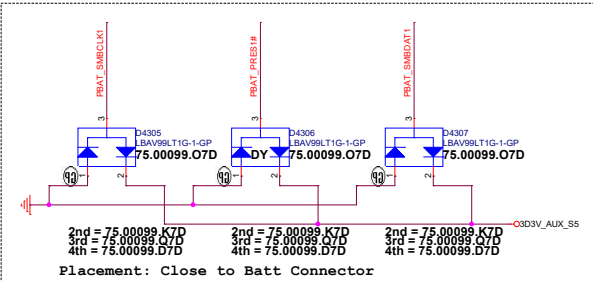
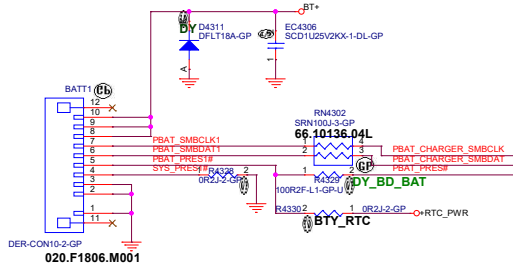
3

2

1

Main Func = BATT Com

## Batt Connector



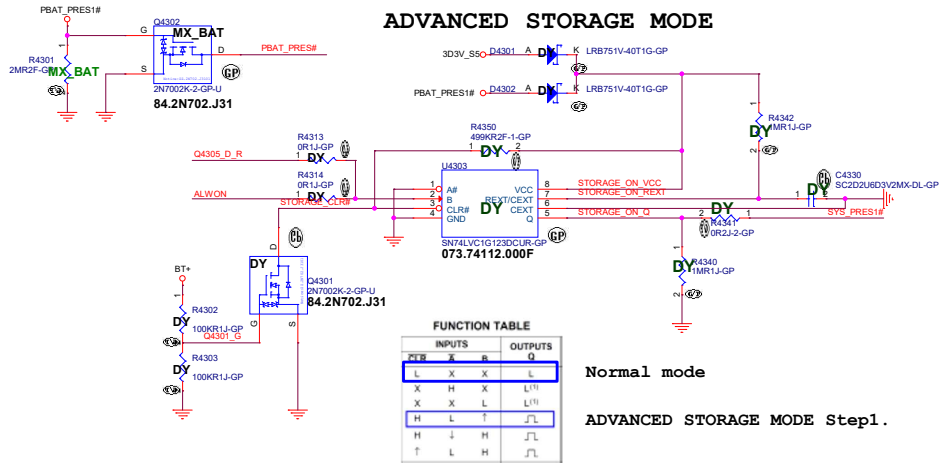
Close BATT1 (p.43)




```

96 PBAT_SMBCLK1
96 PBAT_SMBDAT1

```

## ADVANCED STORAGE MODE

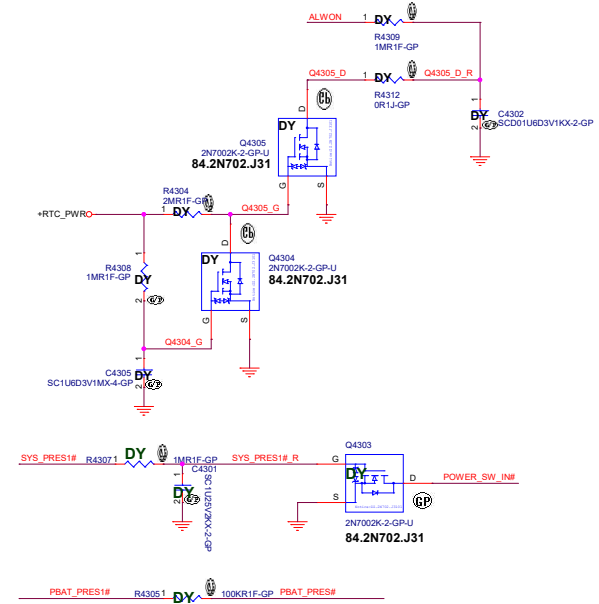


INPUTS			OUTPUTS
P	X	R	Q
L	X	X	L
X	H	X	L <sup>(1)</sup>
X	X	L	L <sup>(1)</sup>
H	L	↑	
H	↓	H	
↑	L	H	

Normal mode

ADVANCED STORAGE MODE Step1.

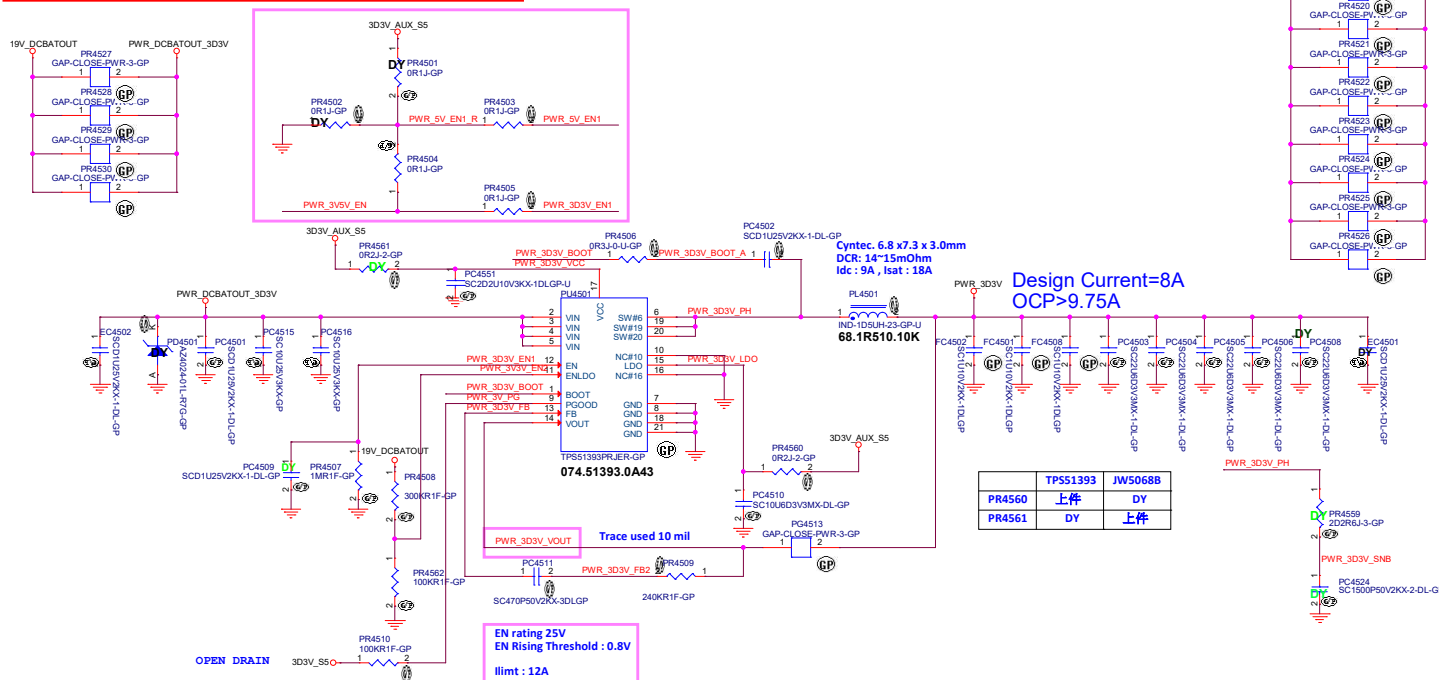
## Press power button duration time improvement



<https://vinafix.com>



**Main Func = Power System 5V/3D3V**

[illegible]

## OFFPAGE

6 SVID\_DATA\_CPU >>> SVID\_DATA\_CPU  
6 SVID\_CLK\_CPU >>> SVID\_CLK\_CPU  
6 SVID\_ALERT#\_CPU >>> SVID\_ALERT#\_CPU

24.44 VR\_EN >>>

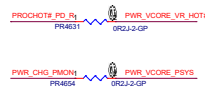
PH on CPU side  
PWR\_VCORE\_VR\_RDY <<< PWR\_VCORE\_VR\_RDY  
PWR\_VCORE\_VR\_HOT# <<< PWR\_VCORE\_VR\_HOT#

PROCHOT#\_PD\_R  
PWR\_VCORE\_FB <<< PWR\_VCORE\_FB  
PWR\_VCORE\_COMP <<< PWR\_VCORE\_COMP

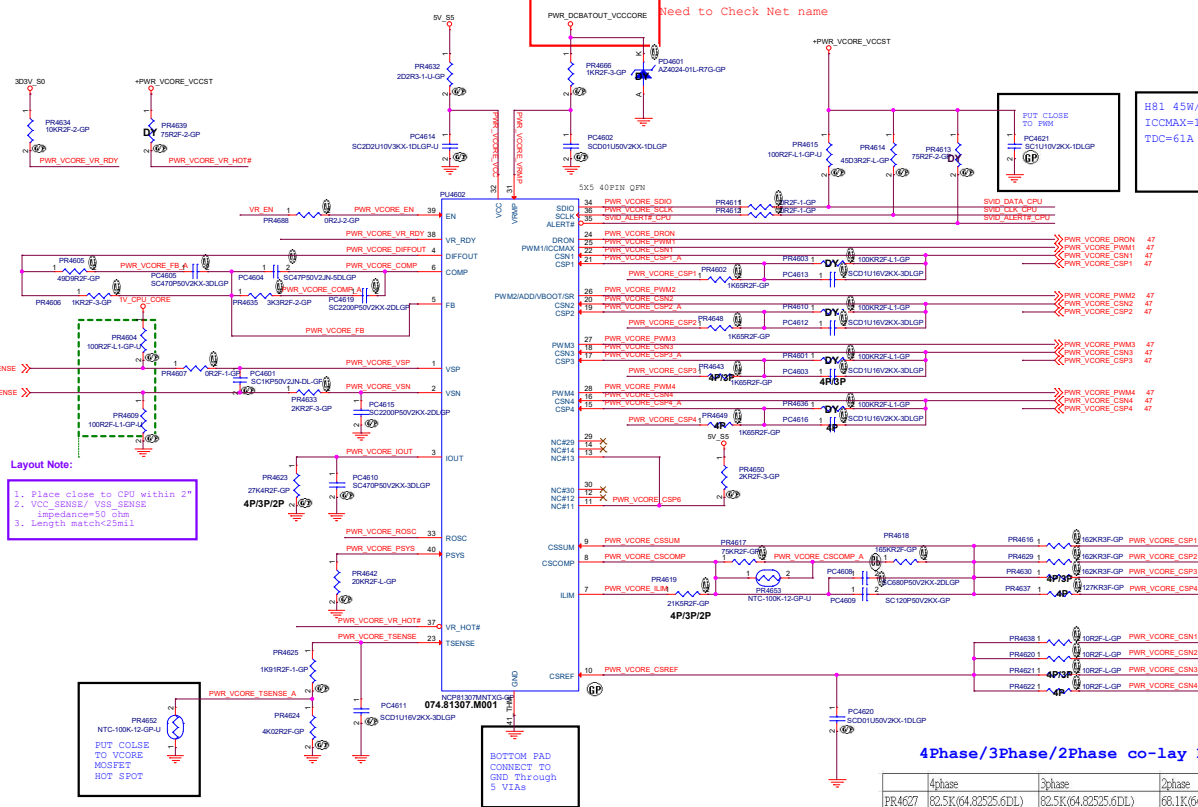
VCCORE\_SENSE <<< VCCORE\_SENSE  
VSSCORE\_SENSE <<< VSSCORE\_SENSE

VSSCORE\_SENSE <<< VSSCORE\_SENSE

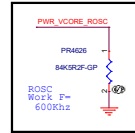
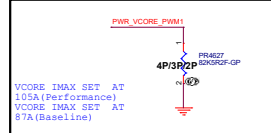
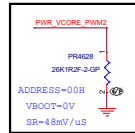
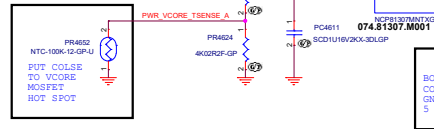
44 PWR\_CHG\_PMON <<< PWR\_CHG\_PMON



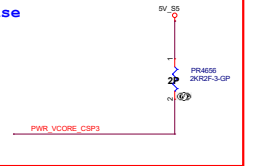
## Tigerlake IMVP9 Power - H-line 45W 4 phase



Layout Note:  
1. Place close to CPU within 2"  
2. VCC\_SENSE/ VSS\_SENSE  
impedance=50 ohm  
3. Length match=25mm



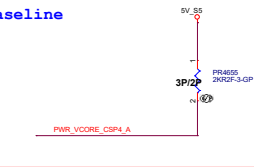
For 2Phase



H81 45W/Performance line  
ICCMAX=105A  
TDC=61A

H81 45W/Base line  
ICCMAX=87A  
TDC=51A

For Baseline



## 4Phase/3Phase/2Phase co-lay Bom

	4phase	3phase	2phase
PR4627	82.5K(64.82525.6DL)	82.5K(64.82525.6DL)	66.1K(64.66125.6DL)
PR4649	1.65K(64.16515.6DL)	DY	DY
PC4616	0.1uF(78.10421.2FLDL)	DY	DY
PR4619	21.5K(64.21525.6DL)	21.5K(64.21525.6DL)	17.8K(64.17825.6DL)
PR4637	127K(64.12735.5SL)	DY	DY
PR4655	DY	2K(64.20015.6DL)	2K(64.20015.6DL)
PR4623	26.1K(64.26125.6DL)	26.7K(64.26725.6DL)	26.7K(64.26725.6DL)
PR4643	1.65K(64.16515.6DL)	1.65K(64.16515.6DL)	DY
PC4603	0.1uF(78.10421.2FLDL)	0.1uF(78.10421.2FLDL)	DY
PR4630	127K(64.12735.5SL)	127K(64.12735.5SL)	DY
PR4656	DY	DY	2K(64.20015.6DL)
PR4622	10R(64.10R05.6DL)	DY	DY
PR4621	10R(64.10R05.6DL)	10R(64.10R05.6DL)	DY

43 PWR\_VCORE\_CSN1 PWR\_VCORE\_

43 PWR\_VCORE\_CSN1 PWR\_VCORE\_

43 PWR\_VCORE\_CSN2 PWR\_VCORE\_

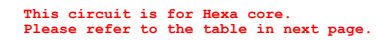
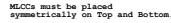
43 PWR\_VCORE\_CSN2 PWR\_VCORE\_

43 PWR\_VCORE\_CSN3 PWR\_VCORE\_

43 PWR\_VCORE\_CSN3 PWR\_VCORE\_

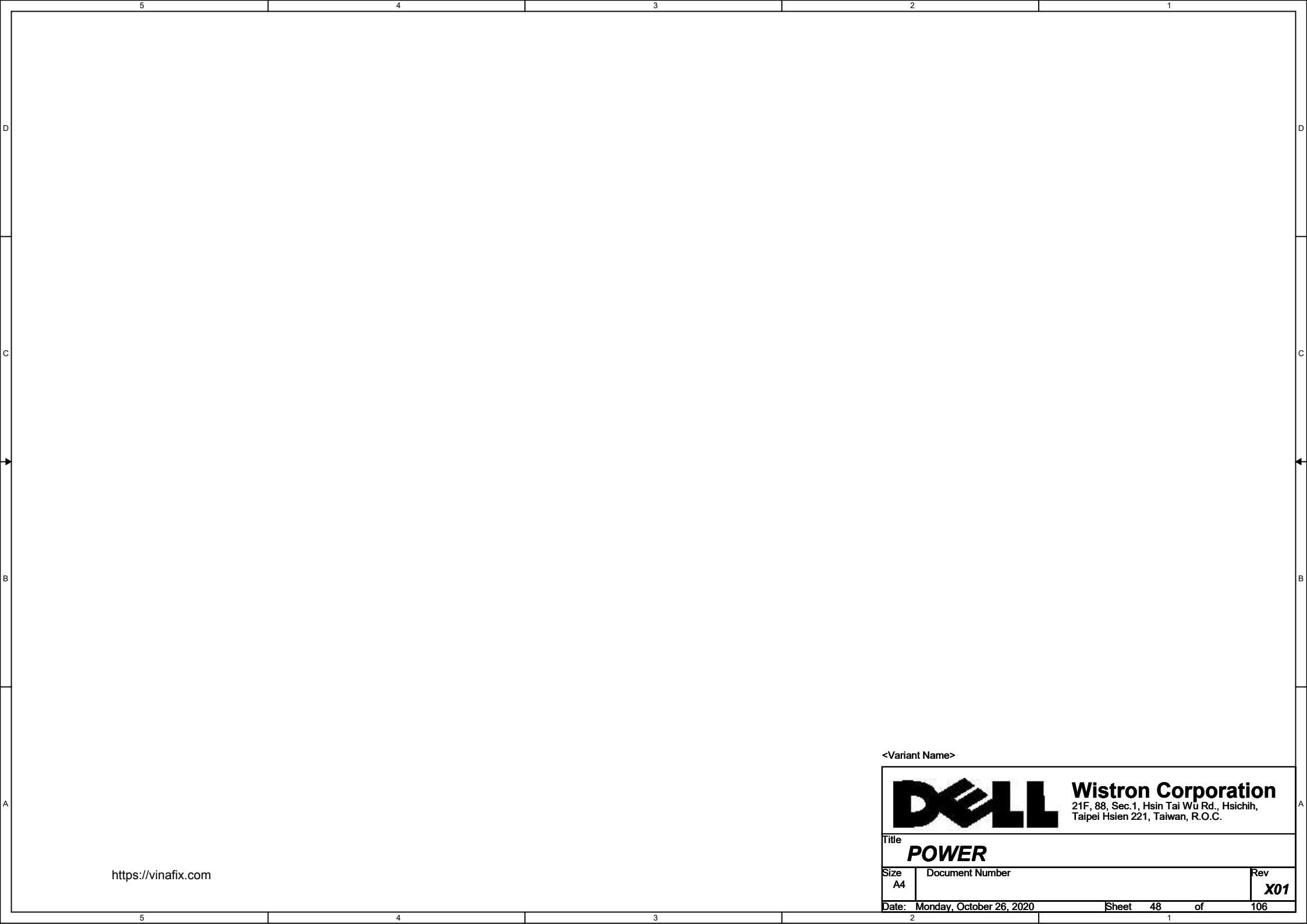
43 PWR\_VCORE\_CSN4 PWR\_VCORE\_

43 PWR\_VCORE\_CSN4 PWR\_VCORE\_




 <b>Wistron Corporation</b> <small>215, 8th, Sec. 2, Taoyuan City, Taoyuan, Taiwan, R.O.C.</small>	
<b>Power (NCP302155A_CPUCORE(2/3))</b>	
<b>Model:</b> <small>See system identifier...</small> <b>Case:</b> <b>Broadmoor 15 TGL-H</b>	<b>Part No.:</b> <b>X91</b>
<b>Manufacturer:</b> <b>Cybernet AS, Wistron</b>	<b>Manufacturer:</b> <b>27 of 124</b>





<https://vinafix.com>


<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>POWER</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 48 of	106

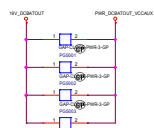
5	4	3	2	1
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<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>NCP81210MN_CPU_VCCGTUS</b>		
Size A4	Document Number	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 49 of 106

## OFFPAGE GAP

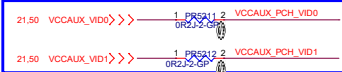




**Main Func = VCCIN\_AUX**

## OFFPAGE

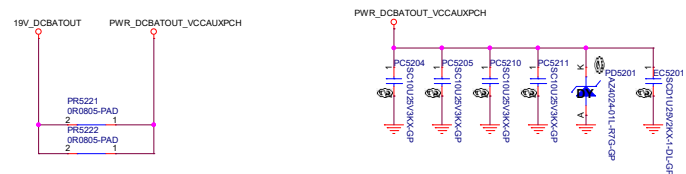
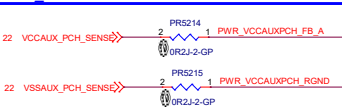
VID



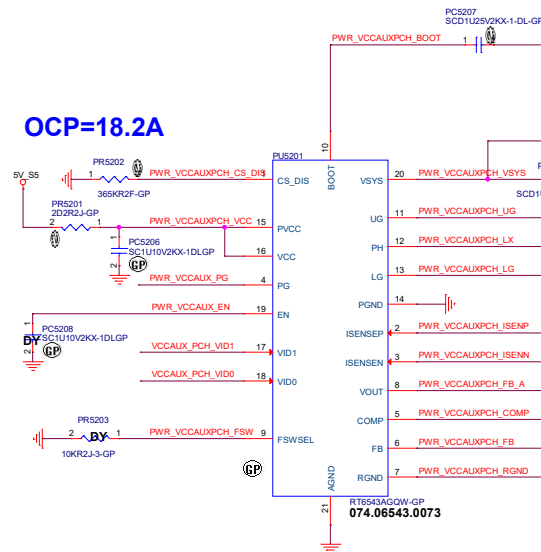
50 PWR\_VCCAUX\_EN &gt;&gt;

40,50 PWR\_VCCAUX\_PG &lt;&lt;&lt;-

**VCCIN\_AUX SENSE**

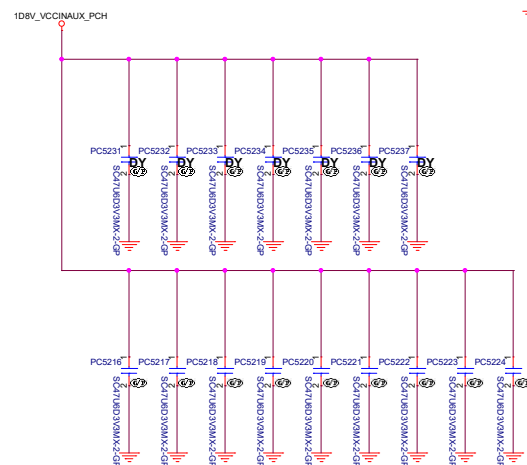


**OCP=18.2A**



TGL-H 42 45W  
TDC=7A  
ICCMAX=13A

Cyntec. 4.8mm x4.7mmx 3.0mm  
DCR: 3.5~3.9m Ohm  
Idc : 14A , Isat : 14.5A



Power Rail	Decap Placement	Form Factor	Value	Number
VCCIN_AUX_PCH	Primary Side	0603	47uF	5
	Primary Side	0402	10uF	4
	Primary Side	0603	47uF	2

<https://vinafix.com>

<Variant Name>

**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

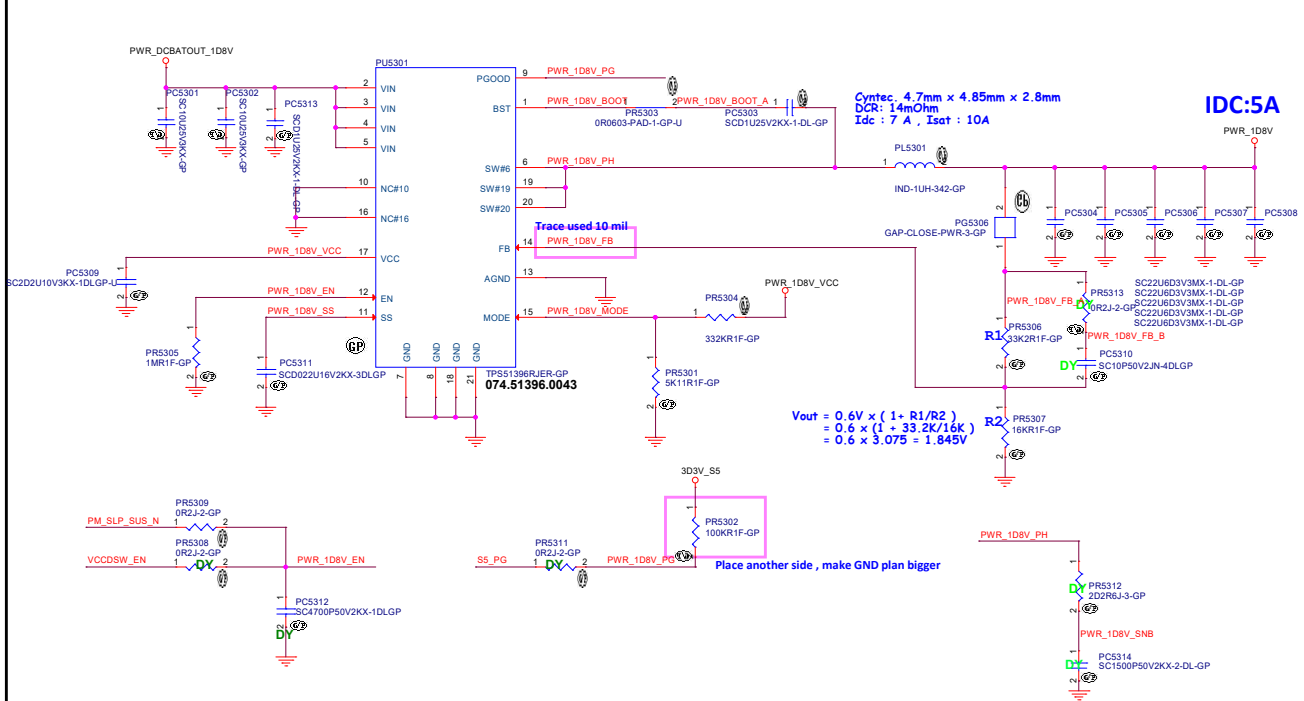
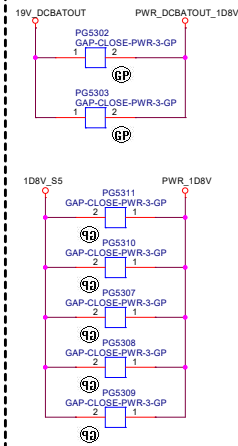
Title **RT6543A VCCAUXPCH**

Size A2	Document Number	Rev X01
Date: Monday, October 26, 2020	Sheet 52 of	106

# OFFPAGE-Signal

18 PM\_SLP\_SUS\_N >>>  
24.40 VCCDSW\_EN >>>  
24.40 SS\_PG <<<  
50 PWR\_1D8V\_PG <<<

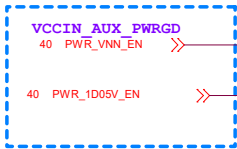
# OFFPAGE-GAP



<https://vinafix.com>

## OFFPAGE

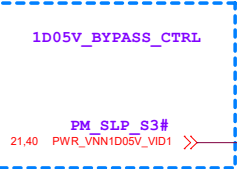
PH on EE Side



PWR\_VNN\_EN

PWR\_1D05V\_EN

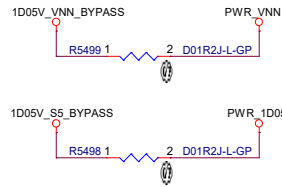
PH on EE Side



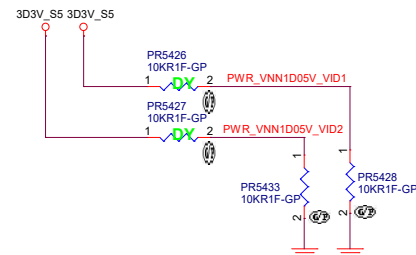
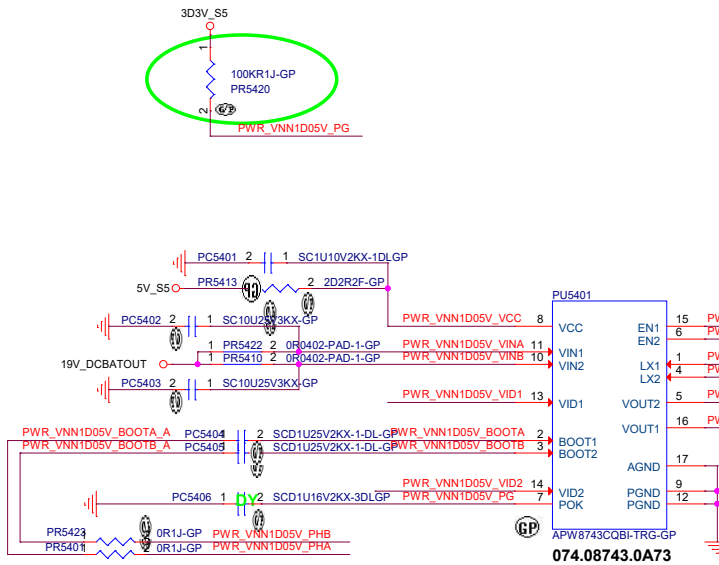
PWR\_VNN1D05V\_VID1

40 PWR\_VNN1D05V\_PG <<<<

## OFFPAGE-GAP

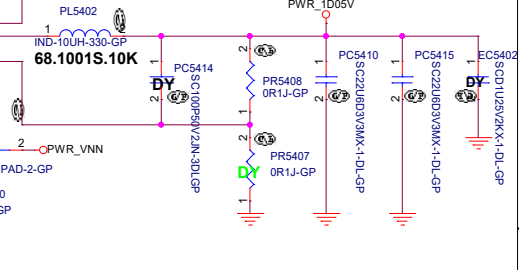


VID1 VNN OUTPUT VOLTAGE	
1	0.78 V
0	1.05 V
VID2 V1P05 OUTPUT VOLTAGE	
1	0.96 V
0	1.05 V



Murata. 2.7mm×2.2mmX1.2mm  
DCR: 59m Ohm  
Idc : 3A, Isat : 3A

Murata. 2.7mm×2.2mmX1.2mm  
DCR: 460m Ohm  
Idc : 0.85A, Isat : 1A

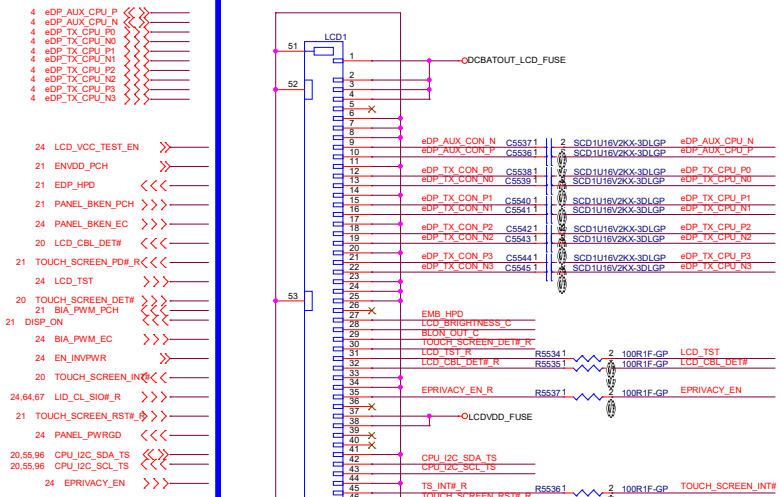


<Variant Name>

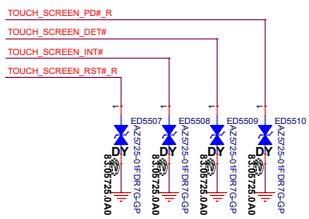
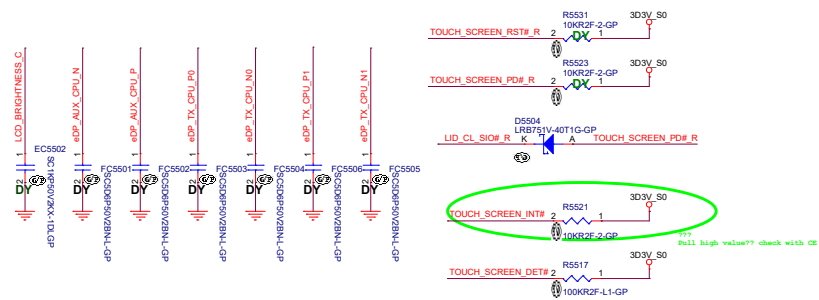
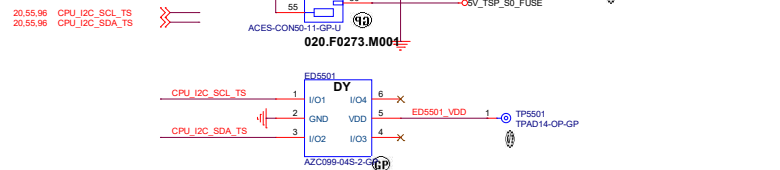
<b>緯創資通 Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>APW8738_ByPASS</b>	
Title Size Custom	Document Number <b>Broadmoor 15 TGL-H</b>
Date Monday, October 26, 2020	Sheet 54 of 106
Rev <b>X01</b>	



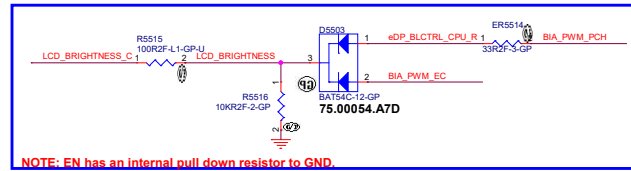
Main Func = LCD/Touch



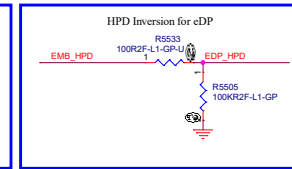
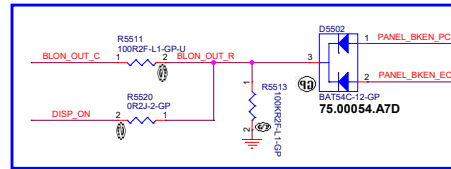
Close LCD1 (p.55)



<https://vinafix.com>

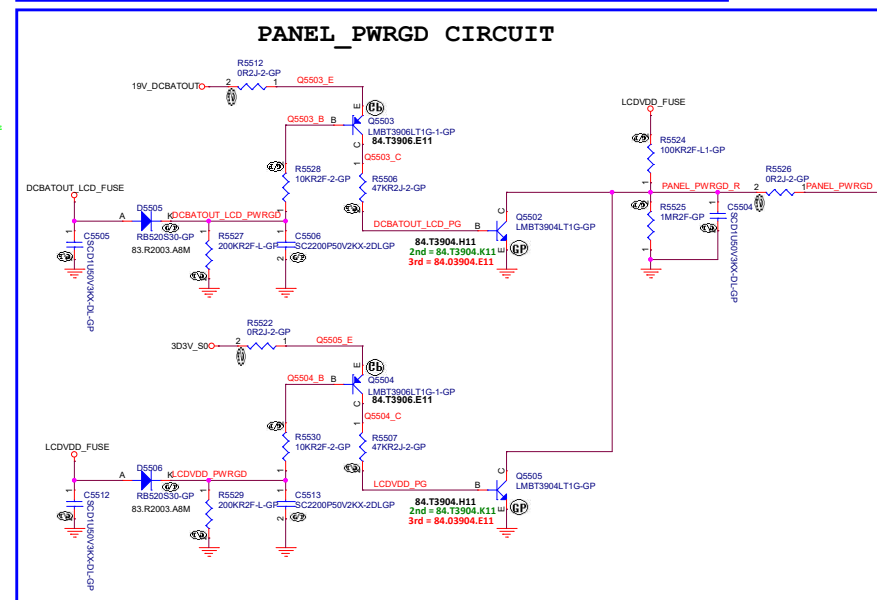
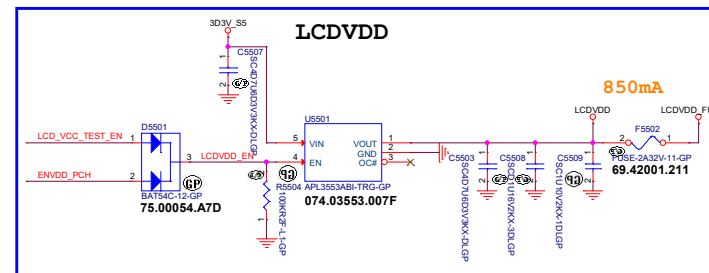
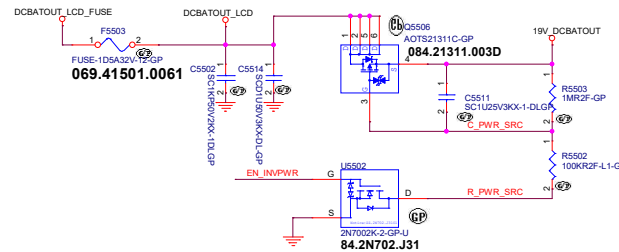


**NOTE: EN has an internal pull down resistor to GND**



1086mA

### INVERTER POWER



<Variant Name>



Titolo	<b>Display (LCD/Inverter)</b>
--------	-------------------------------

Size A2	Document Number	Rev X0
------------	-----------------	-----------

# Main Func = IR CAM

18 CCD\_USB20\_N  
18 CCD\_USB20\_P  
27 DMIC\_SDA\_CODECCON  
27 DMIC\_SCL\_CODECCON  
21 IR\_CAM\_DET#  
20 CAM\_MIC\_CBL\_DET#

21,56,96 P\_CLK  
21,56,96 P\_DATA

20 P\_SENSOR\_DET#

21 ISH\_ALS\_INT#

20 SECURE\_BIO

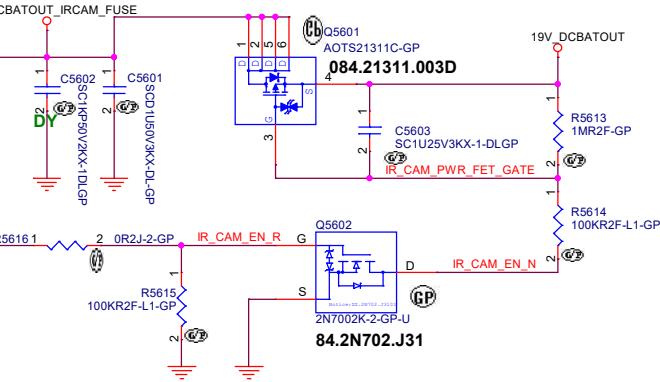
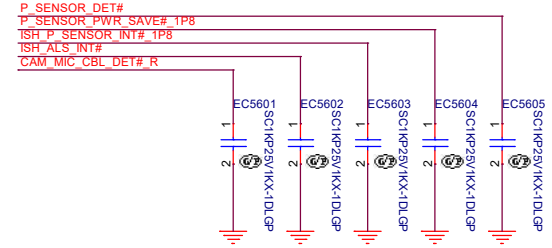
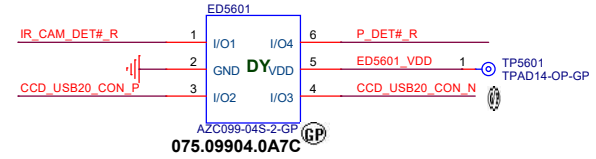
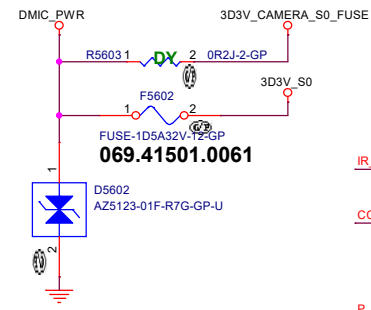
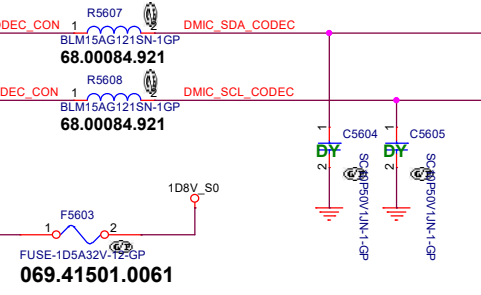
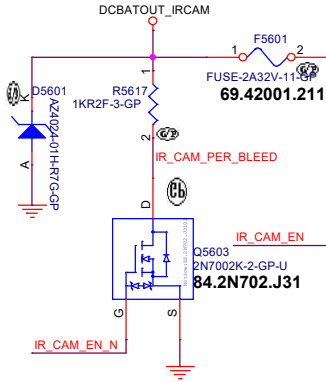
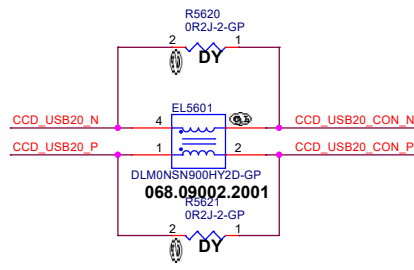
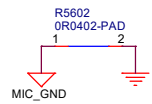
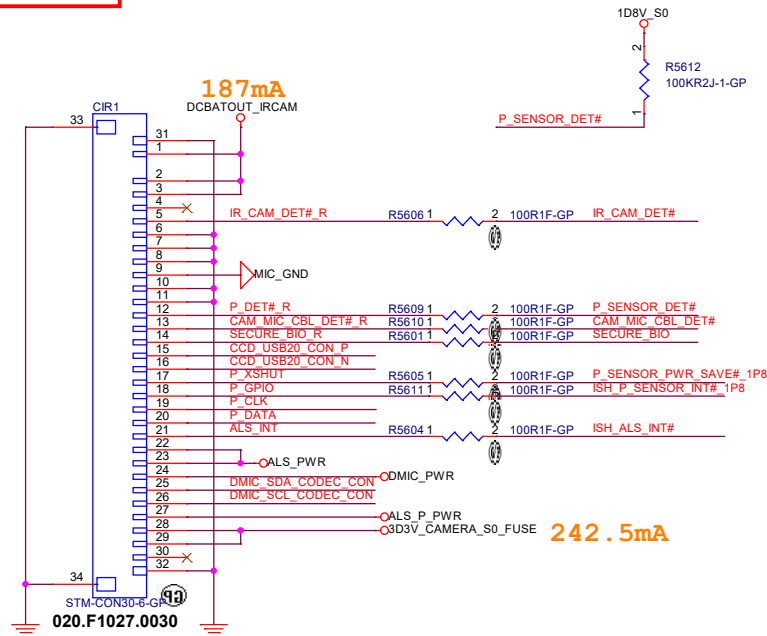
20 P\_SENSOR\_PWR\_SAVE#\_1P8

21 ISH\_P\_SENSOR\_INT#\_1P8

24 IR\_CAM\_EN

Close CIR1 (p.56)

21,56,96 P\_CLK  
21,56,96 P\_DATA




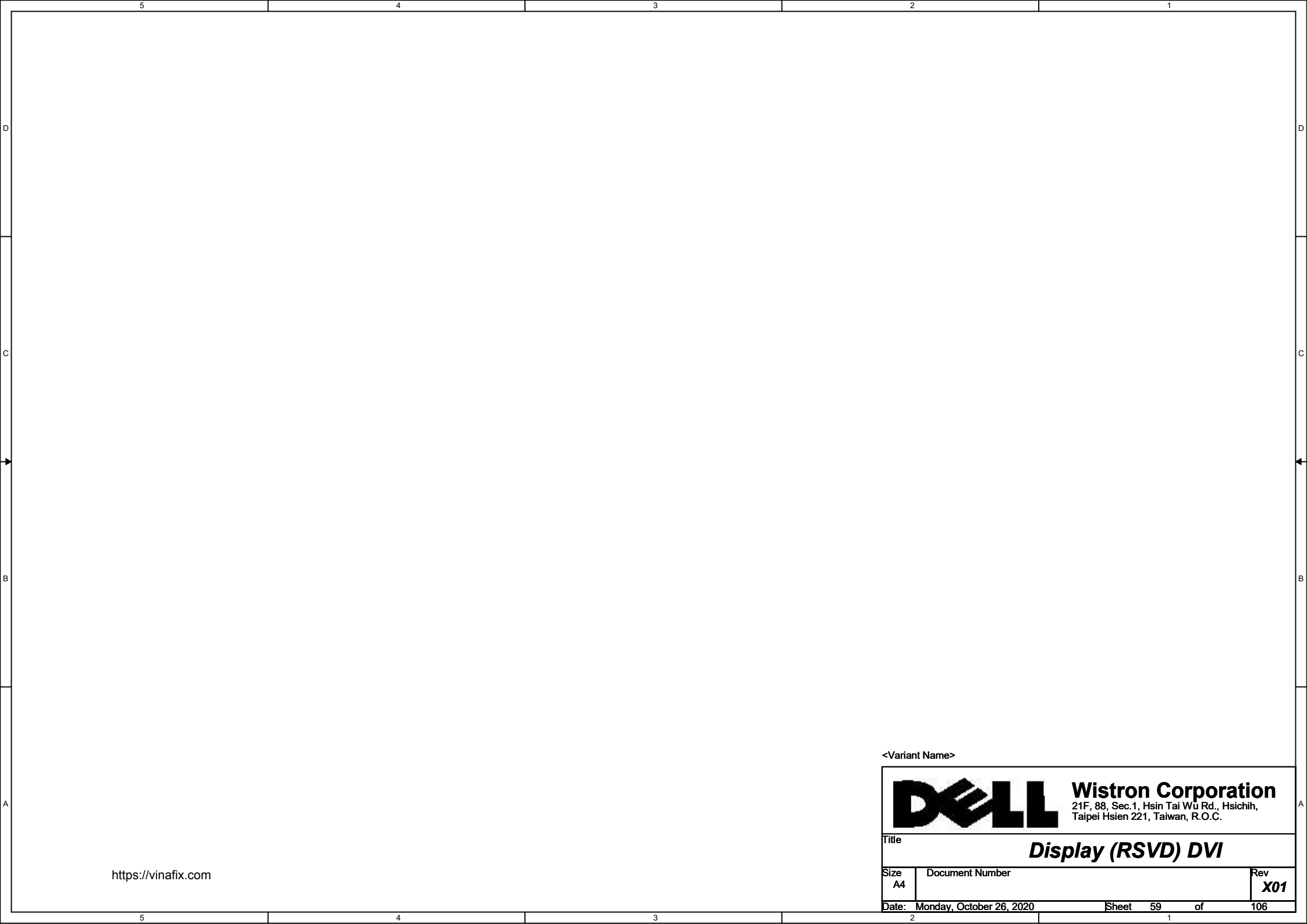


5	4	3	2	1
D				
C				
B				
A				

<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Display (RSVD) DP</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020	Sheet 58	of	106



D

D

C

C

B


B

A

A

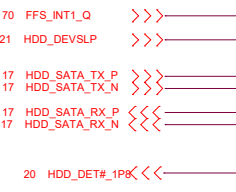
<https://vinafix.com>

<Variant Name>

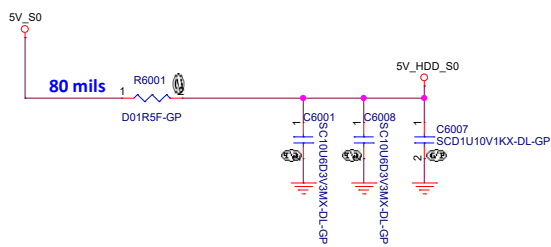
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Display (RSVD) DVI</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020	Sheet	59	of 106

SSID = HDD

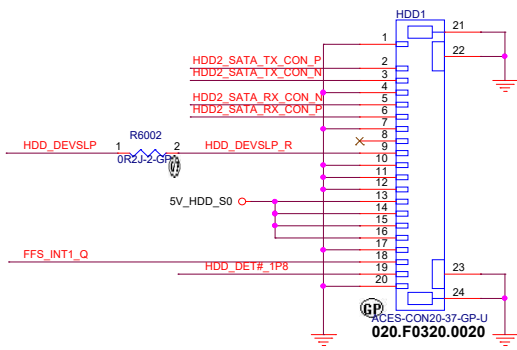
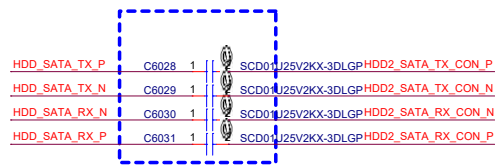
HDD



HDD POWER



SATA HDD Connector



<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Size Custom Document Number Rev  
**SATA IF HDD/ODD**  
**Broadmoor 15 TGL-H** X01

Date: Monday, October 26, 2021 Sheet 60 of 106

# Main Func = WLAN

## WLAN

17 WLAN\_PCIE\_RX\_N  
17 WLAN\_PCIE\_RX\_P  
17 WLAN\_PCIE\_TX\_N  
17 WLAN\_PCIE\_TX\_P

## BT

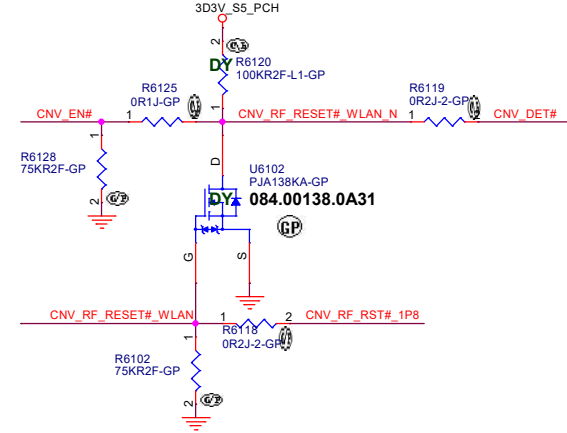
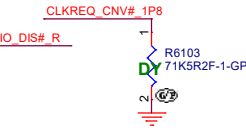
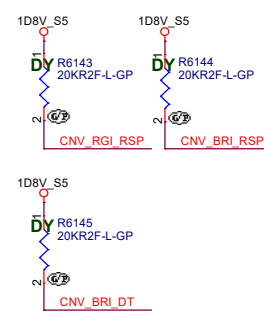
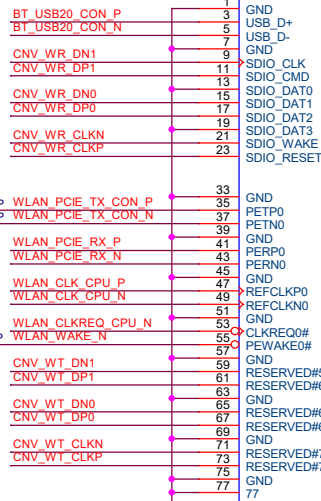
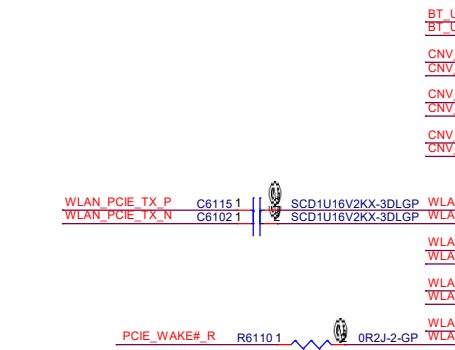
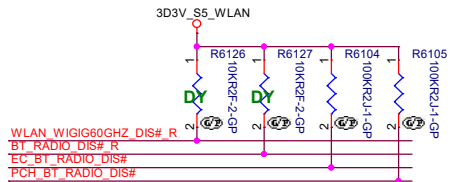
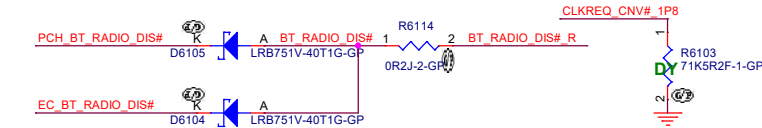
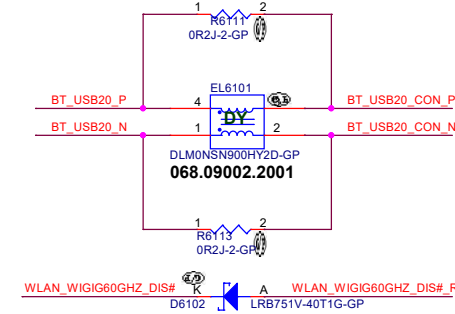
18 BT\_USB20\_N  
18 BT\_USB20\_P

## CNVi

19 CNV\_WR\_DN1  
19 CNV\_WR\_DP1  
19 CNV\_WR\_DN0  
19 CNV\_WR\_DP0  
19 CNV\_WR\_CLKN  
19 CNV\_WR\_CLKP  
19 CNV\_WT\_DN1  
19 CNV\_WT\_DP1  
19 CNV\_WT\_DN0  
19 CNV\_WT\_DP0  
19 CNV\_WT\_CLKN  
19 CNV\_WT\_CLKP  
21 CNV\_BRI\_RSP  
11,21 CNV\_RGI\_DT  
11,21 CNV\_BRI\_DT  
21 CNV\_RGI\_RSP  
20 CNV\_RF\_RST#\_1P8  
24 CNV\_DET#

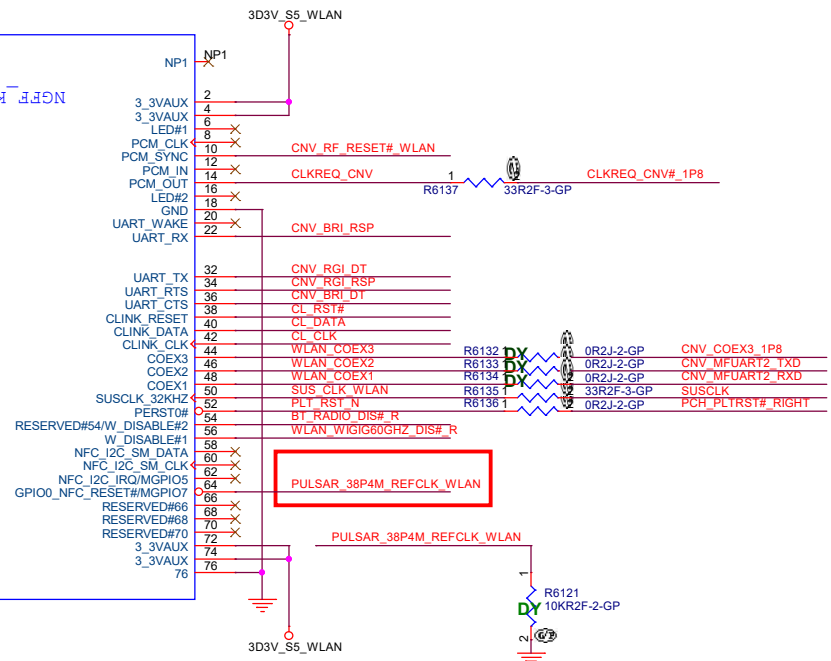
## WLAN

19 WLAN\_CLK\_CPU\_P  
19 WLAN\_CLK\_CPU\_N  
20 WLAN\_CLKREQ\_CPU\_N  
24,62,63 PCIE\_WAKE#\_R  
21,62 CNV\_COEX3\_1P8  
21,62 CNV\_MFUART2\_TXD  
21,62 CNV\_MFUART2\_RXD  
20 CL\_CLK  
20 CL\_DATA  
20 CL\_RST#  
20 CLKREQ\_CNV#\_1P8  
24 WLAN\_WIGIG60GHZ\_DIS#  
24 EC\_BT\_RADIO\_DIS#  
16 SUSCLK  
20,33,62,79,91,97 PCH\_PLTRST#\_RIGHT  
21 CNV\_EN#  
20 PCH\_BT\_RADIO\_DIS#



1090mA

NGFF\_KEY\_E\_75P



<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchi,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INT IO (WLAN M.2)**

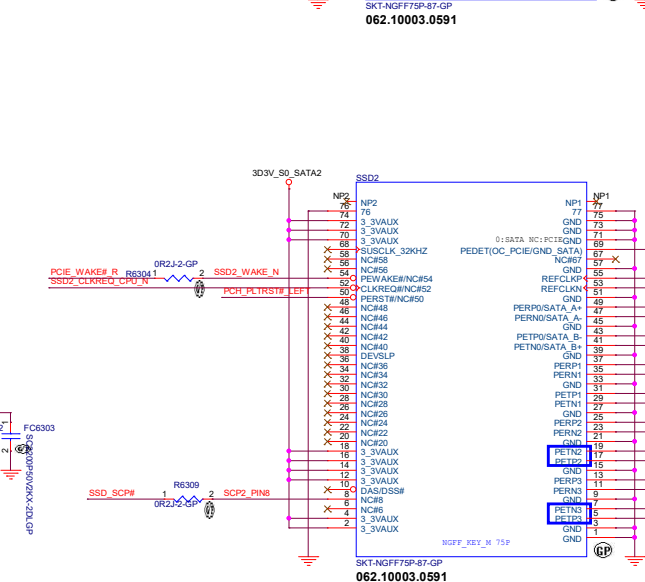
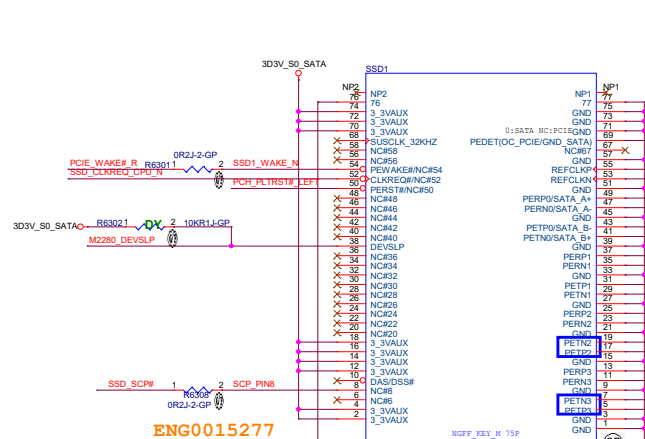
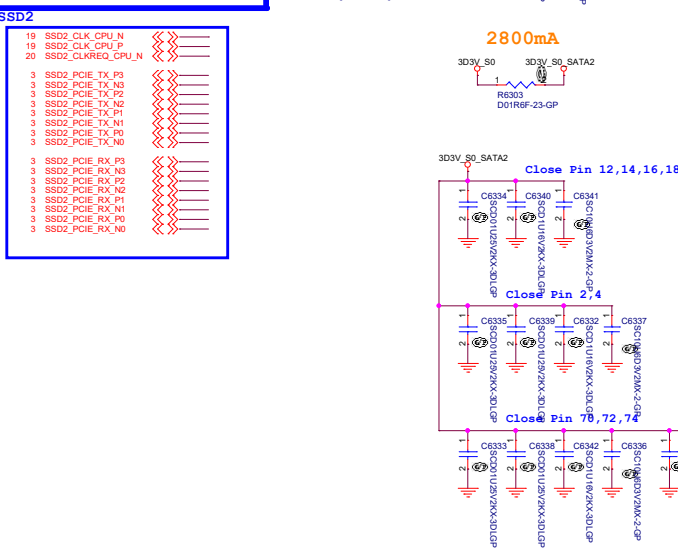
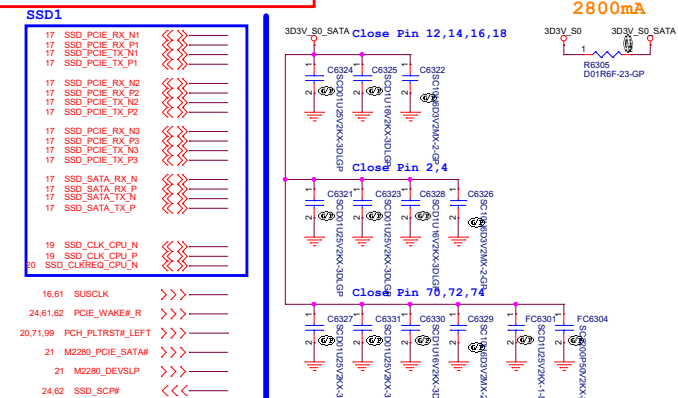
Size: A3 Document Number: X01

Date: Monday, October 26, 2020 Sheet: 61 of 106





**Main Func = m.2 SSD**



PEDET	0	Host I/F Indication: To be grounded for SATA, No Connect for PCIE	0V
-------	---	--	----

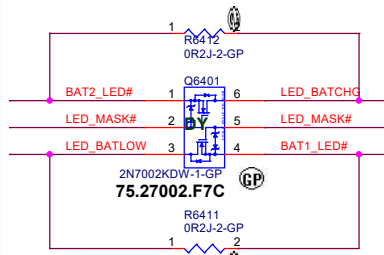
  

L	SATA
H	PCIE

72	3 V	GND	75
73	3 V	GND	73
74	3 V	GND	73
68	SUSCLK(32MHz) (IO/3 V)	PEDET (NC-PGM/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GND	57
	N/C	REFCLK	55
54	PEWAKE(1/10V 3 V) or N/C	REFCLK	55
52	CLKREQ(1/10V 3 V) or N/C	GND	51
50	PERST(0 V/3 V) or N/C	PETP/VSATA-A-	49
	N/C	PETNP/VSATA-A+	47
44	N/C	GND	43
42	N/C	PERP/VSATA-B-	43
40	N/C	PERNP/VSATA-B+	41
38	DEVSLP (O)	GND	39
36	N/C	PETP1	37
34	N/C	PETN1	35
32	N/C	GND	33
30	N/C	PERP1	31
28	N/C	PERN1	29
26	N/C	GND	27
24	N/C	PETP2	25
22	N/C	PETN2	23
20	N/C	GND	21
18	3 V	PERP2	19
16	3 V	PERN2	17
14	3 V	GND	15
12	3 V	PETP3	13
10	3 V	PERP3	11
	DAS/DSS# (1/10V LED+ LED-) (3 V)	GND	9
8	N/C	PERP3	7
6	N/C	PERN3	5
4	3 V	GND	3
2	3 V	GND	1

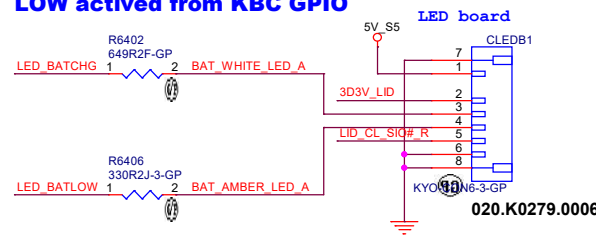
# Main Func = LED/HALL/Button

24 BAT2\_LED# >>>  
 24 BAT1\_LED# >>>  
 24,32 LED\_MASK# >>>  
 24,68 KBC\_PWRBTN# <<<  
 24,55,64,67 LID\_CL\_SIO#\_R <<<  
 92 MASK\_BASE\_LEDS#\_Q <<<  
 24 POWER\_ON\_LED# <<<  
 24,92 FPR\_DET# >>>  
 24 M\_BIST >>>  
 24,44 ACAV\_IN >>>  
 16,17,24,99 RSMRST#\_KBC >>>  
 67 3D3V\_LID >>>  
 24,55,64,67 LID\_CL\_SIO#\_R >>>

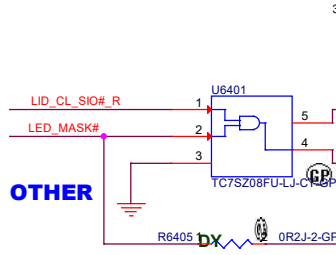


Stealth mode

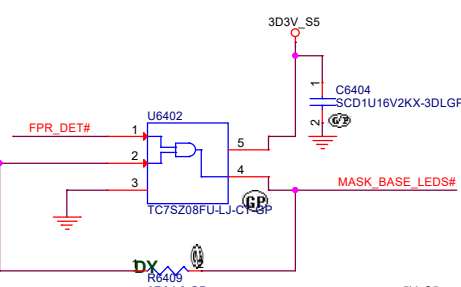
## Battery LED2(White LED) LOW acted from KBC GPIO



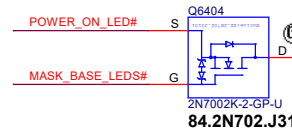
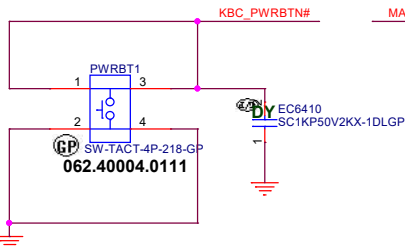
## Battery LED1(Orange LED) LOW acted from KBC GPIO



POWERBT

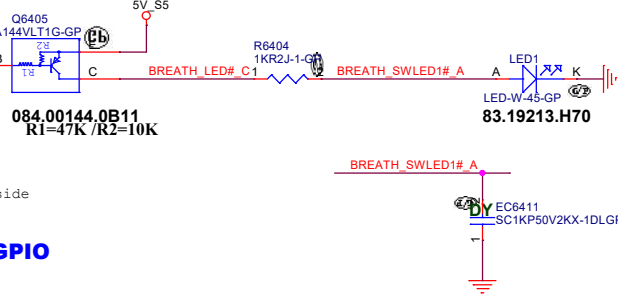


## POWER BUTTON

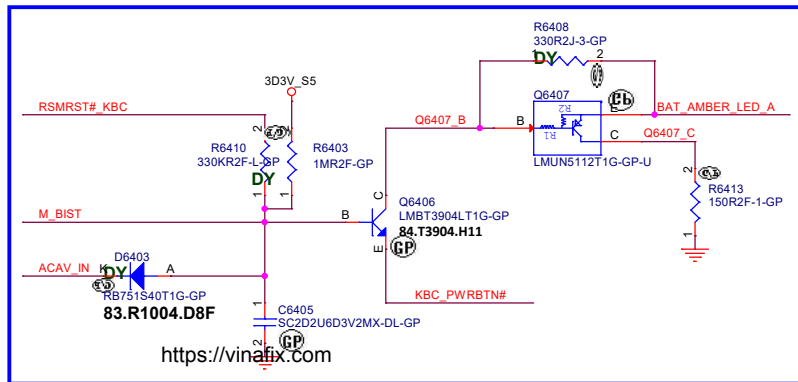


Resistor already reserve on EC side

Power LED  
LOW acted from KBC GPIO



## M-BIST



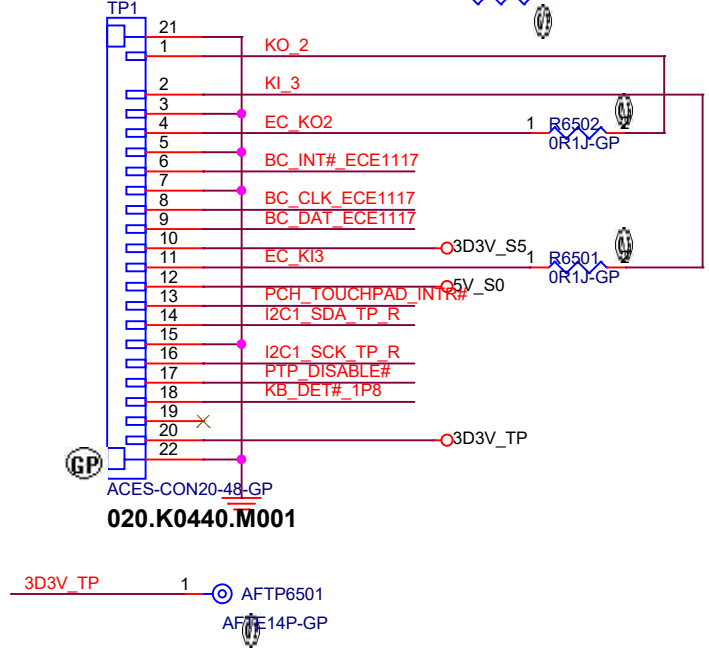
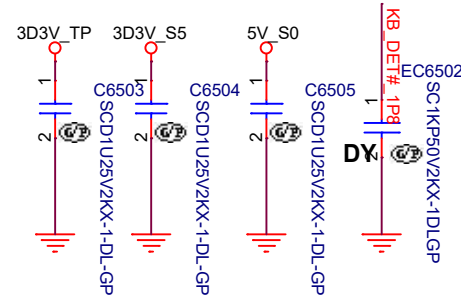
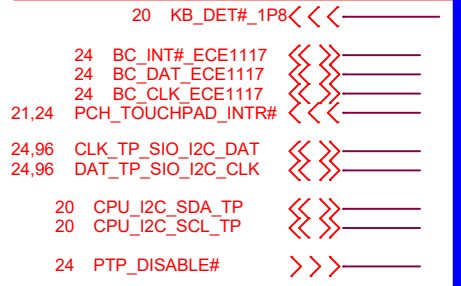
<Variant Name>

**DELL** Wistron Corporation  
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
 Taipei Hsien 221, Taiwan, R.O.C.

LED / Button / Power Button

Size Custom Document Number Rev X01  
 Date: Monday, October 26, 2020 Sheet 64 of 106

# Main Func = Key Board/Touch Pad

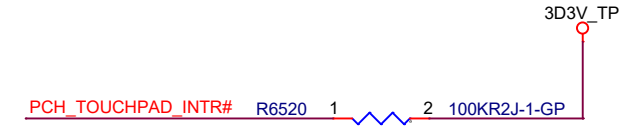
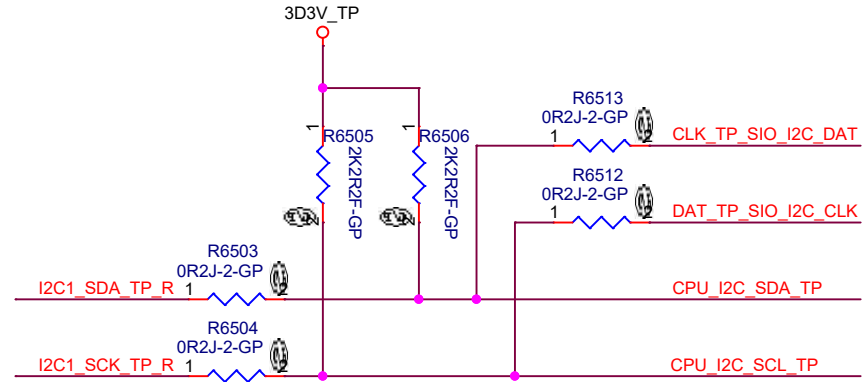
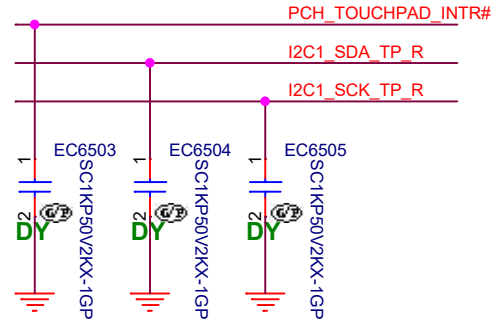
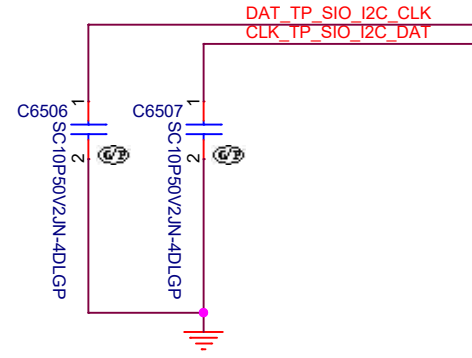


10mA

Close TP1 (p.65)

96 I2C1\_SCK\_TP\_R

96 I2C1\_SDA\_TP\_R



<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
<b>Title</b> <b>INT IO (KB/TP)</b>			
<b>Size</b> A4	<b>Document Number</b>		<b>Rev</b> <b>X01</b>
<b>Date:</b> Monday, October 26, 2020		<b>Sheet</b> 65	<b>of</b> 106

# Main Func = USH BD

## USH

18 USH\_USB20\_N <<<>>>  
18 USH\_USB20\_P <<<>>>

24 CV3\_ON >>>>

24,66,69,96 USH\_EXP\_HDMI\_PS\_SMBCLK <<<>>>  
24,66,69,96 USH\_EXP\_HDMI\_PS\_SMBDAT <<<>>>

24 BCM5882\_ALERT# >>>>

24 USH\_PWR\_STATE# <<<<

20 CONTACTLESS\_DET# <<<<

24 USH\_DET# <<<<

92 FP\_USB20\_USH\_N <<<>>>  
92 FP\_USB20\_USH\_P <<<>>>

92 FP\_RESET# <<<<

24,92 FPR\_SCAN\_INT# >>>>

20 SC\_CAGE\_DET# >>>>

CV3 module	
pin assignment - proposal 2	
NC	
NC	
CV2_ON	
USB20_N from FPR	
USB20_P from FPR	
GND	
GND	
USB20_N to PCH	
USB20_P to PCH	
GND	
USH_EXPANDER_SMBCLK	
USH_EXPANDER_SMBDAT	
BCM5882_ALERT#	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
NC	
+5V_ALW	
+3.3V_RUN	
+5V_RUN	
USH_RST#	
USH_PWR_STATE#	
CONTACTLESS_DET#	
GND	
GND	
USH_DET#	

SC\_CAGE\_DET#

FP\_RESET#

CV3\_ON

FP\_USB20\_USH\_N

FP\_USB20\_USH\_P

USH\_USB20\_CON\_N

USH\_USB20\_CON\_P

USH\_EXP\_HDMI\_PS\_SMBCLK

USH\_EXP\_HDMI\_PS\_SMBDAT

BCM5882\_ALERT#

3D3V\_S5

5V\_S5

3D3V\_S0

5V\_S0

FPR\_SCAN\_INT#

USH\_PWR\_STATE#

CONTACTLESS\_DET# USH

CONTACTLESS\_DET#

USH\_DET#

USH\_DET#\_R

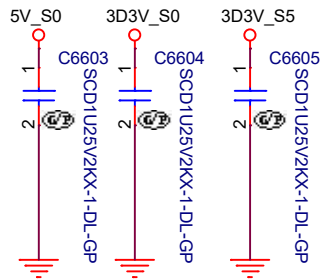
D6602  
LRB751V-40T1G-GP

R6607  
0R2J-2-GP

D6601  
LRB751V-40T1G-GP

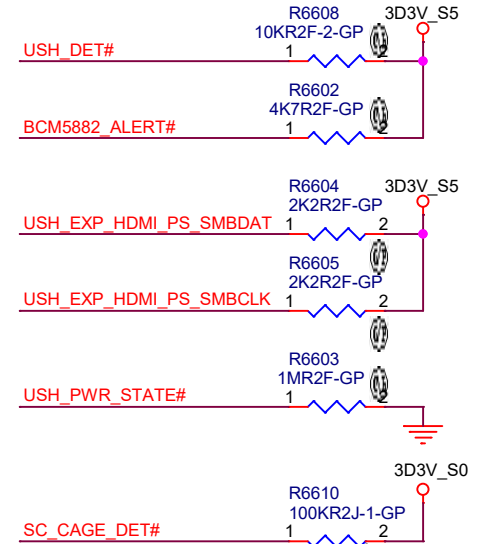
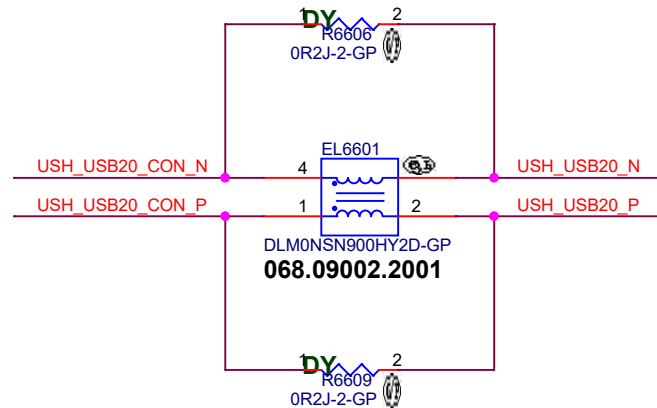
ACES-CONN26-4-GP

020.K0440.M002



## Close USH1 (p. 66)

24,66,69,96 USH\_EXP\_HDMI\_PS\_SMBCLK >>>>  
24,66,69,96 USH\_EXP\_HDMI\_PS\_SMBDAT >>>>



<Variant Name>



**Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**IO Board Conn (USH)**

Size  
A4 Document Number

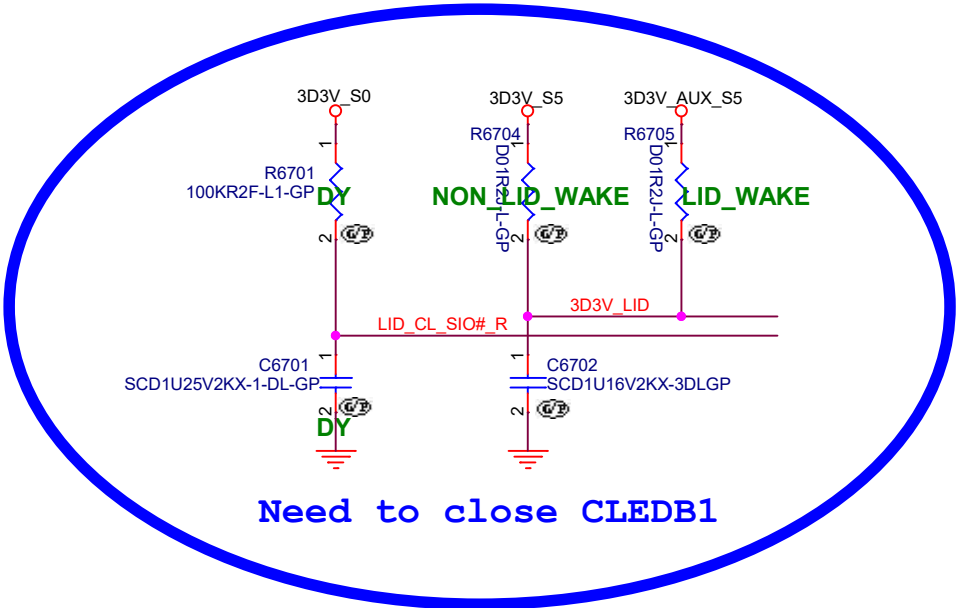
Rev  
**X01**

Date: Monday, October 26, 2020

Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)

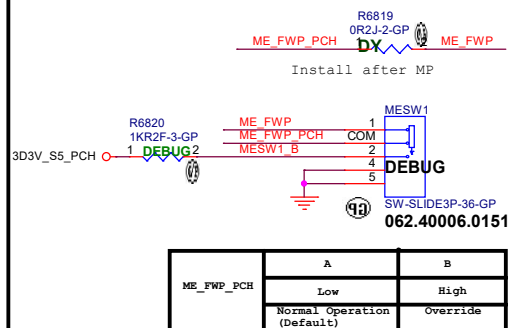
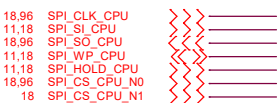
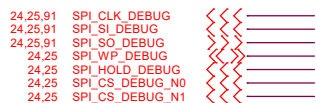
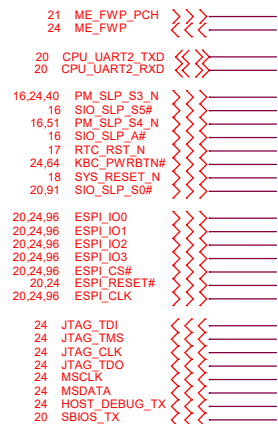
24,55,64 LID\_CL\_SIO#\_R << >>—  
64 3D3V\_LID <<<—



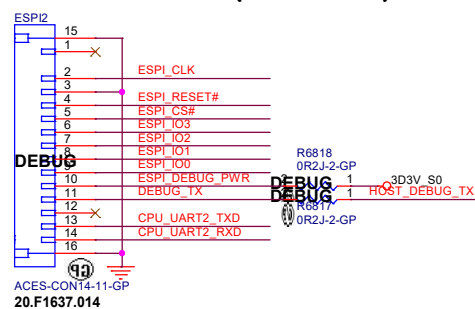
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>Sensor (Hall-Sensor)</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 67 of	106

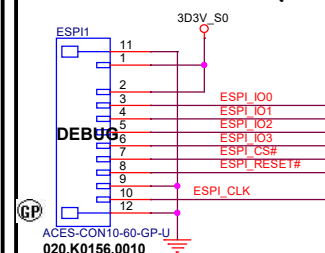
## Main Func = Debug



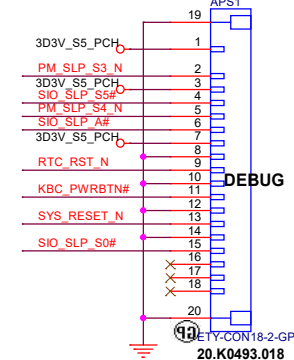
## ESPI DEBUG (Wistron)



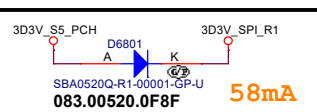
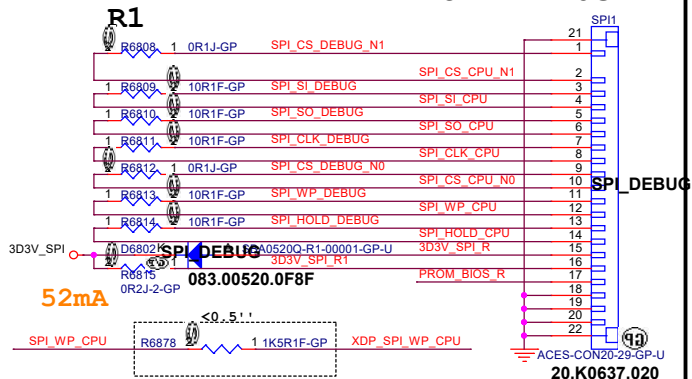
ESPI DEBUG (DELL)



## APS DEBUG

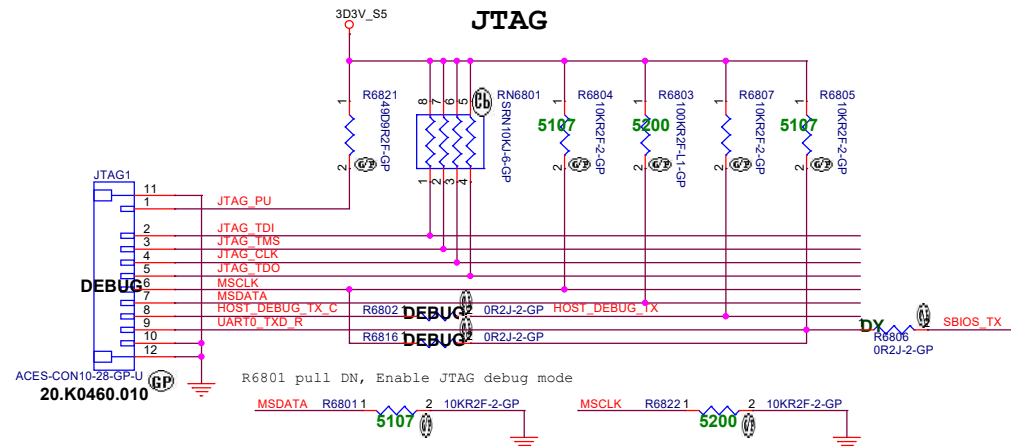


## SPI DEBUG



MP change to short pad

## JTAG



<Variant Name>



**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

114

### **Debug (LPC debug)**

Size  
A3

Document Number
-----------------

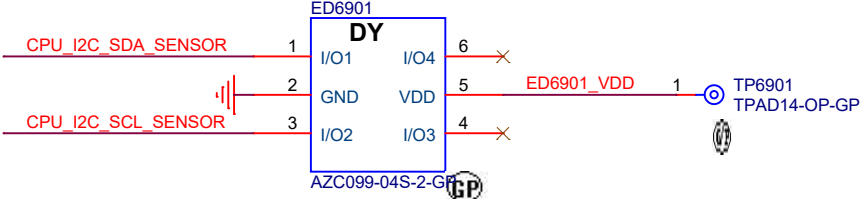
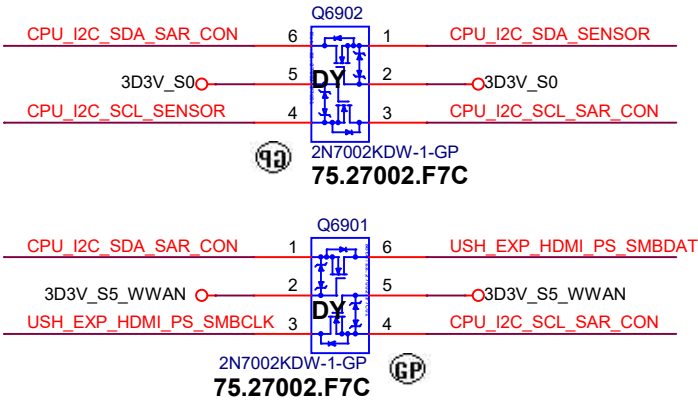
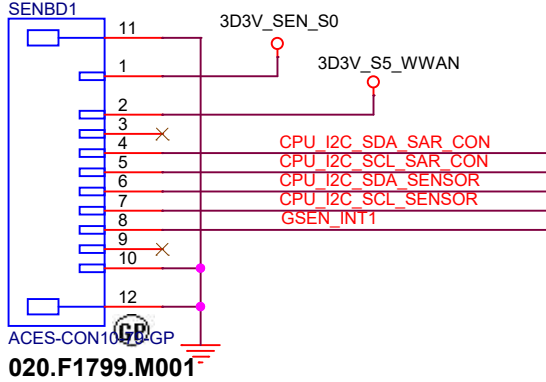
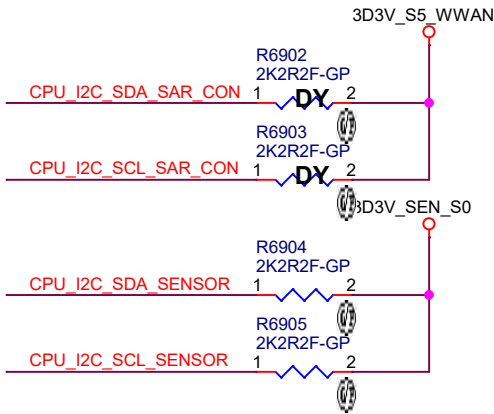
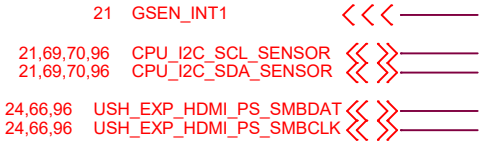
Rev	X01
-----	-----

Date: Monday, October 26, 2020

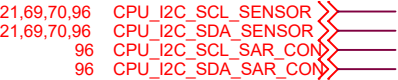
Sheet 6

106

# Main Func = Sensor (E-compass/A+Gyro/SAR)



Close SENBD1(p.69)



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<Variant Name>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b>Sensor (GYROSCOPE/PRESSUE/ALS)</b>			
Size	Document Number		Rev
A4			<b>X01</b>
Date: Monday, October 26, 2020		Sheet 69 of 106	



# Main Func = G-sensor

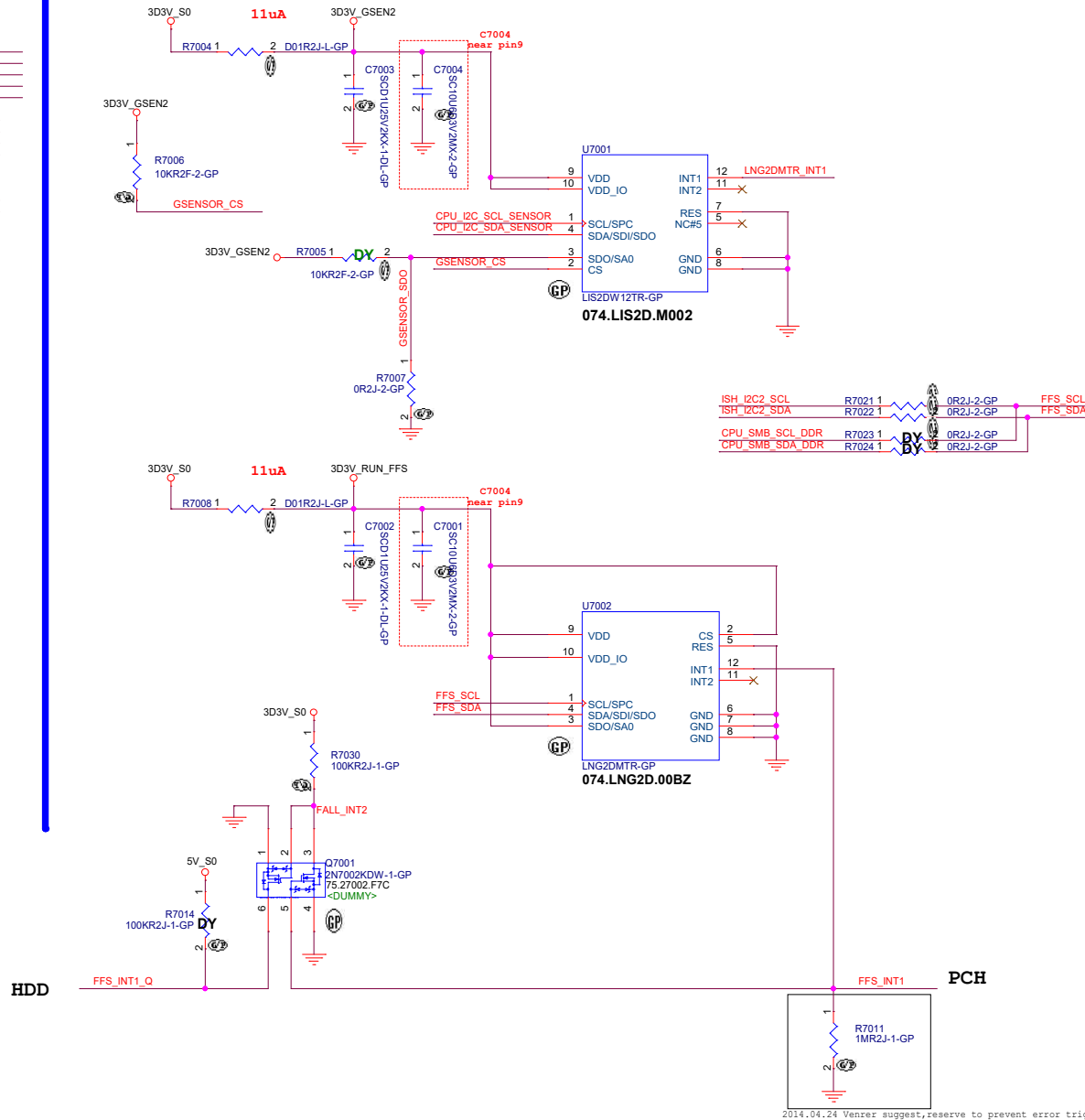
## G Sensor

21,69,70,96 CPU\_I2C\_SDA\_SENSOR  
21,69,70,96 CPU\_I2C\_SCL\_SENSOR  
21 LNG2DMTR\_INT1  
60 FFS\_INT1\_Q  
20 FFS\_INT1

21,24,96 CPU\_SMB\_SCL\_DDR  
21,24,96 CPU\_SMB\_SDA\_DDR  
21,24,96 ISH\_I2C2\_SCL  
21,24,96 ISH\_I2C2\_SDA

Close U7001(P.70)

21,69,70,96 CPU\_I2C\_SCL\_SENSOR  
21,69,70,96 CPU\_I2C\_SDA\_SENSOR



<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

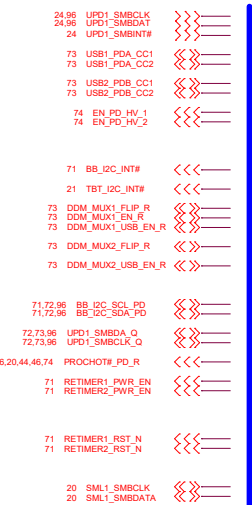
Title **Sensor (G-sensor)**

Size Document Number Rev  
Custom X01

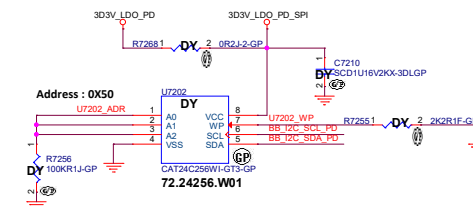
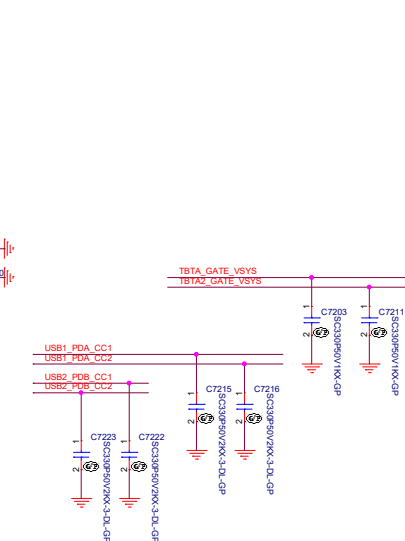
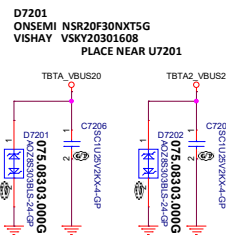
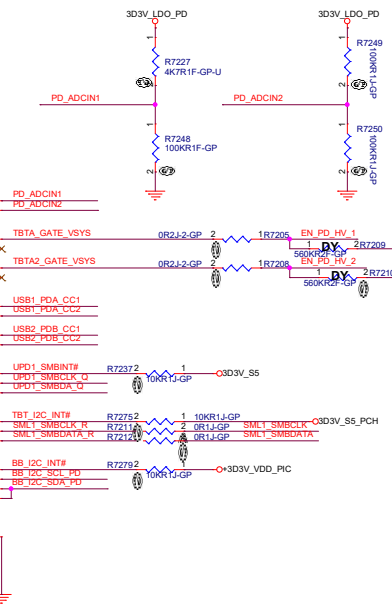
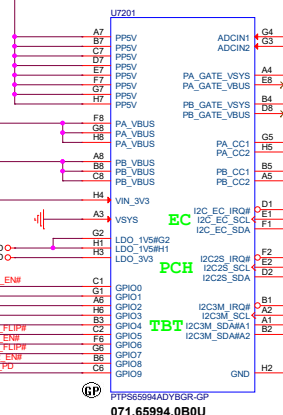
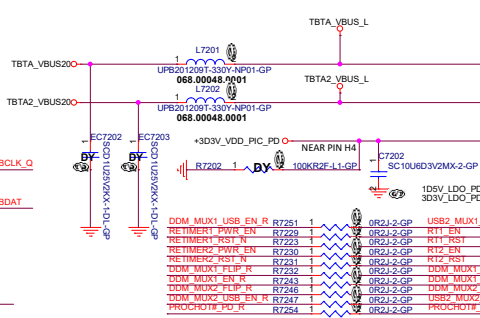
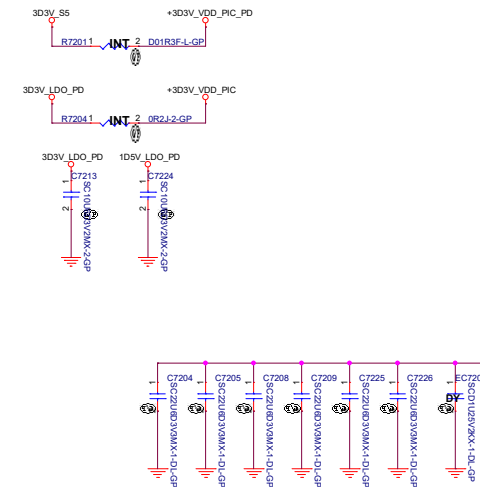
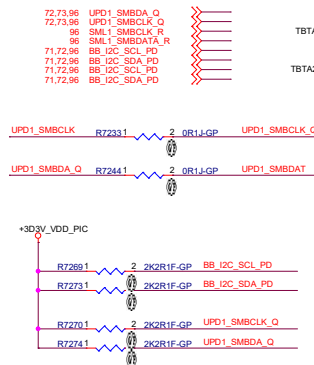
Date: Monday, October 26, 2020 Sheet 70 of 106

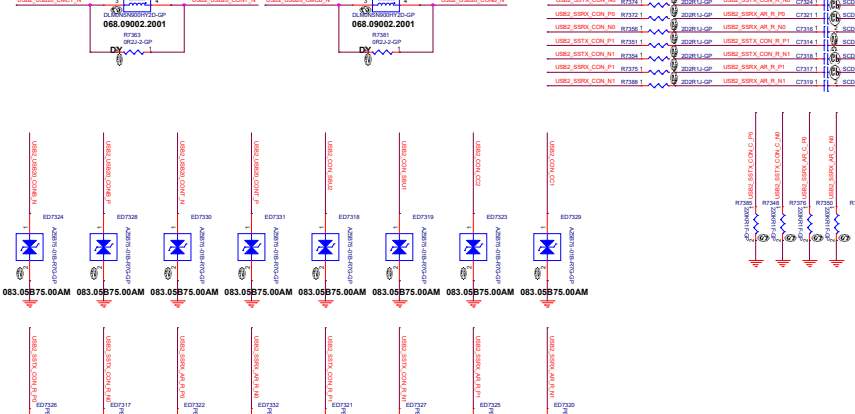
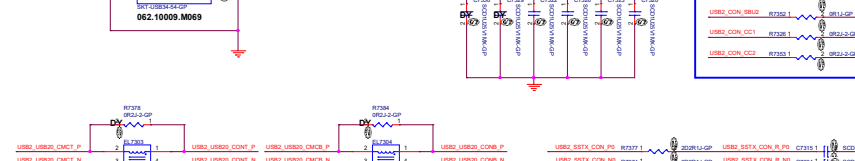
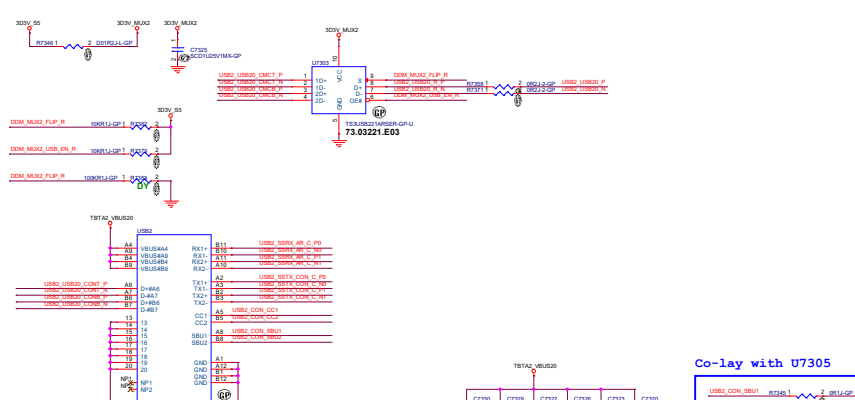
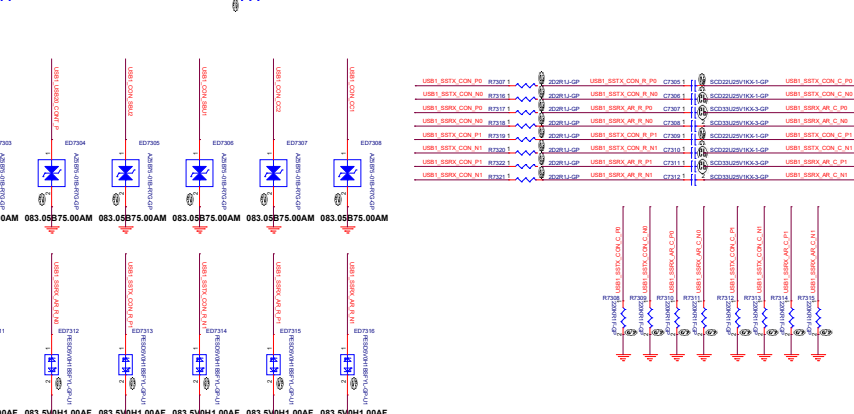
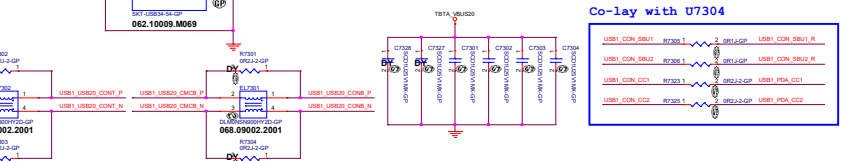
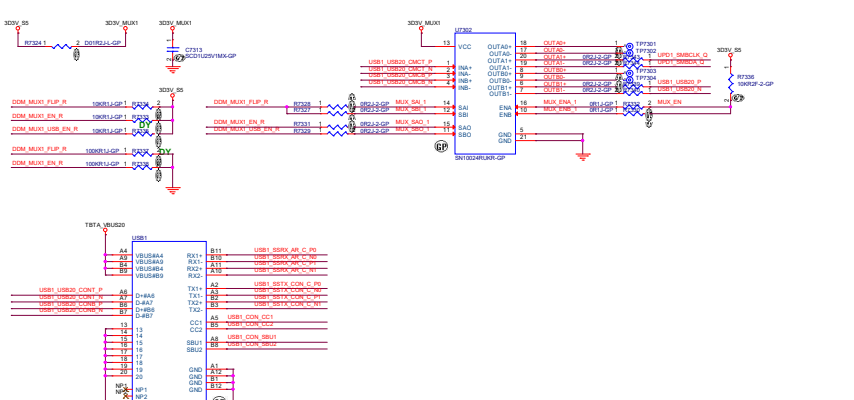


```
Main Func = TypeC
```

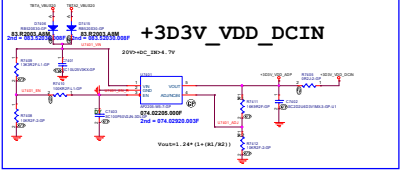
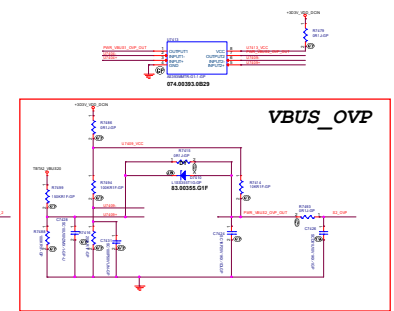
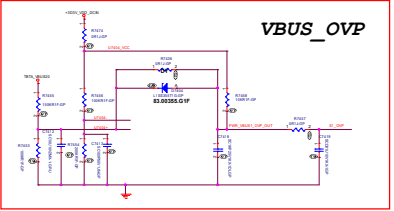
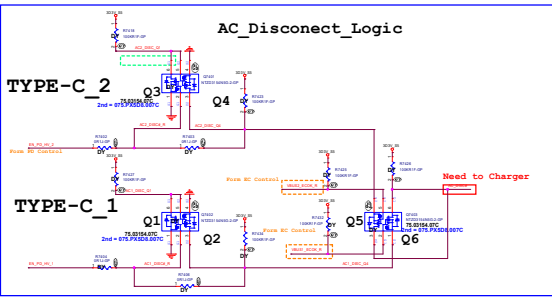
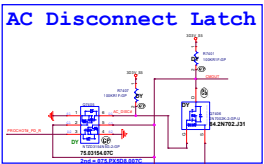


Close U7201 (p.72)

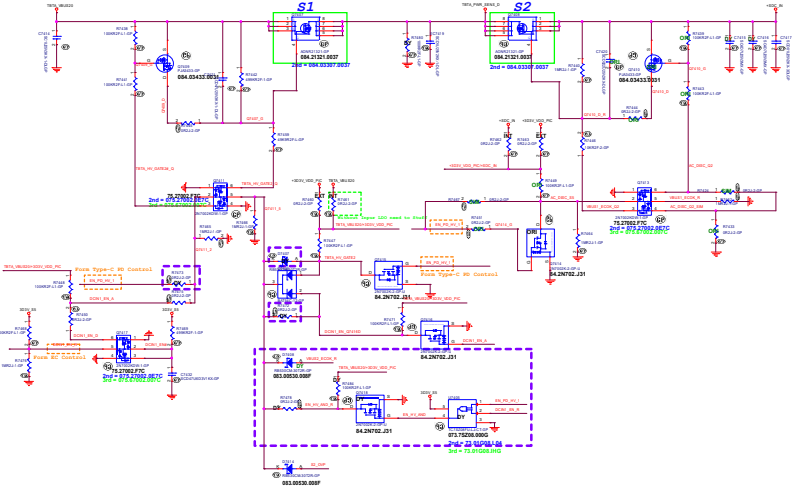


[illegible]

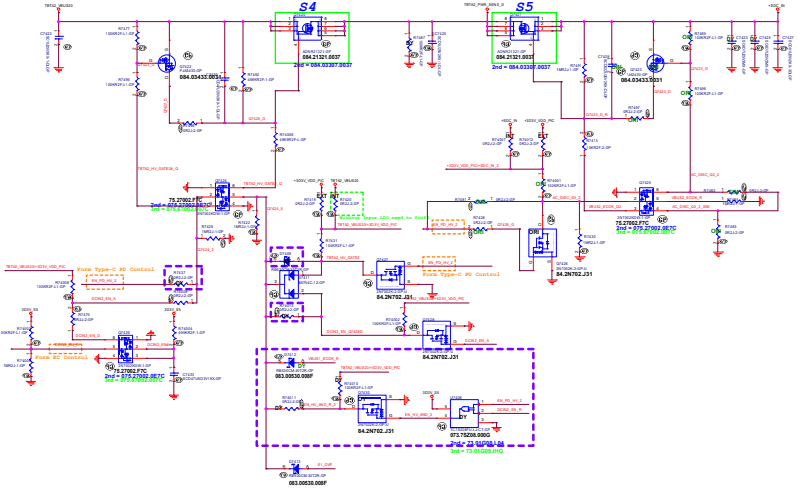
- 1. 100K 1% 0603
- 2. 100K 1% 0603
- 3. 100K 1% 0603
- 4. 100K 1% 0603
- 5. 100K 1% 0603
- 6. 100K 1% 0603
- 7. 100K 1% 0603
- 8. 100K 1% 0603
- 9. 100K 1% 0603
- 10. 100K 1% 0603
- 11. 100K 1% 0603
- 12. 100K 1% 0603
- 13. 100K 1% 0603
- 14. 100K 1% 0603
- 15. 100K 1% 0603
- 16. 100K 1% 0603
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- 18. 100K 1% 0603
- 19. 100K 1% 0603
- 20. 100K 1% 0603
- 21. 100K 1% 0603
- 22. 100K 1% 0603
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- 37. 100K 1% 0603
- 38. 100K 1% 0603
- 39. 100K 1% 0603
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- 41. 100K 1% 0603
- 42. 100K 1% 0603
- 43. 100K 1% 0603
- 44. 100K 1% 0603
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- 46. 100K 1% 0603
- 47. 100K 1% 0603
- 48. 100K 1% 0603
- 49. 100K 1% 0603
- 50. 100K 1% 0603
- 51. 100K 1% 0603
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- 77. 100K 1% 0603
- 78. 100K 1% 0603
- 79. 100K 1% 0603
- 80. 100K 1% 0603
- 81. 100K 1% 0603
- 82. 100K 1% 0603
- 83. 100K 1% 0603
- 84. 100K 1% 0603
- 85. 100K 1% 0603
- 86. 100K 1% 0603
- 87. 100K 1% 0603
- 88. 100K 1% 0603
- 89. 100K 1% 0603
- 90. 100K 1% 0603
- 91. 100K 1% 0603
- 92. 100K 1% 0603
- 93. 100K 1% 0603
- 94. 100K 1% 0603
- 95. 100K 1% 0603
- 96. 100K 1% 0603
- 97. 100K 1% 0603
- 98. 100K 1% 0603
- 99. 100K 1% 0603
- 100. 100K 1% 0603

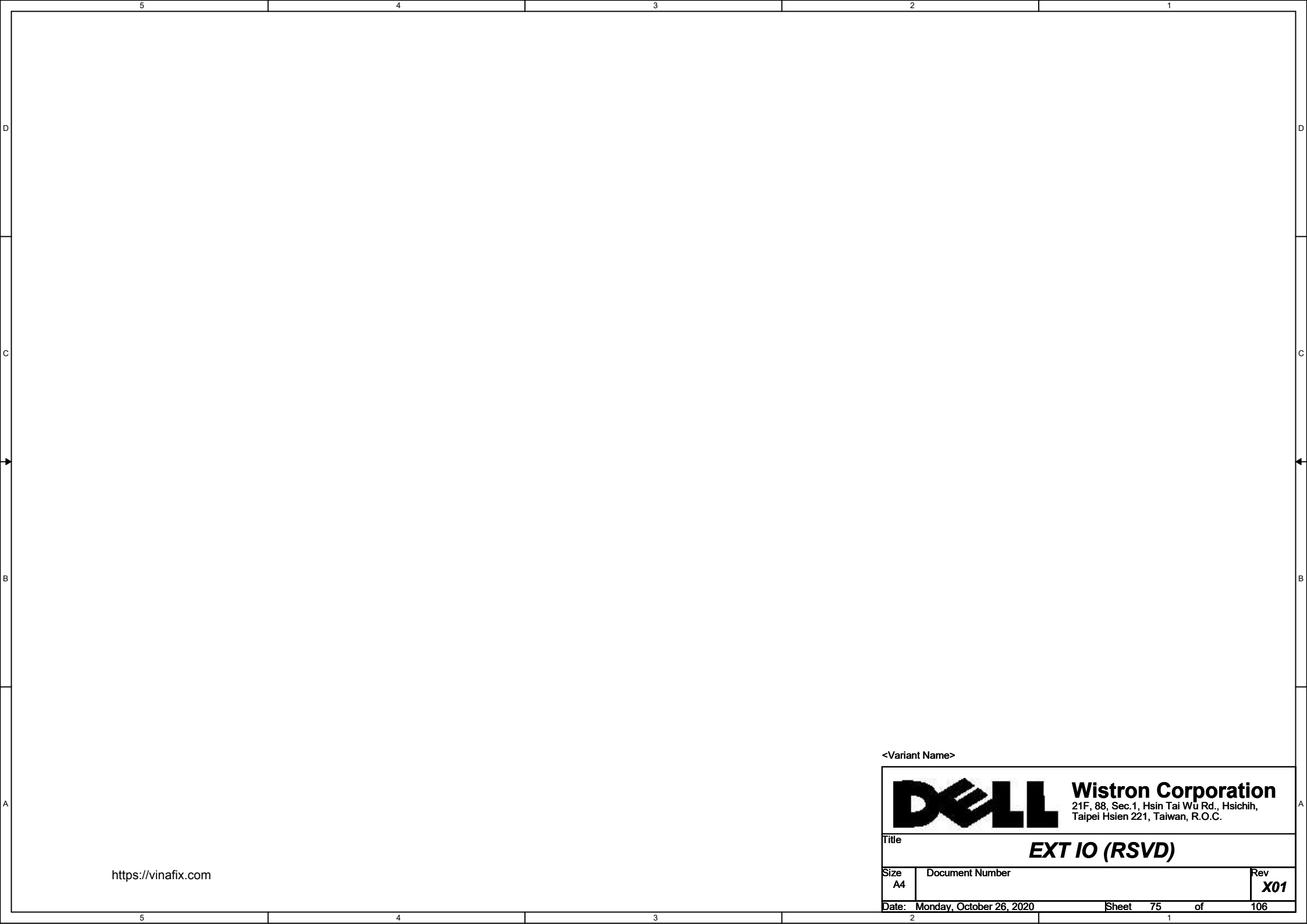


TYPE-C 1



TYPE-C 2





D

D

C

C

B


B

A

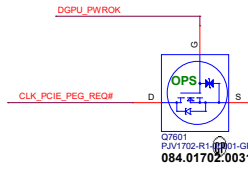
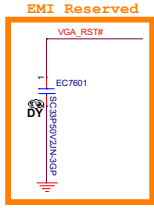
A

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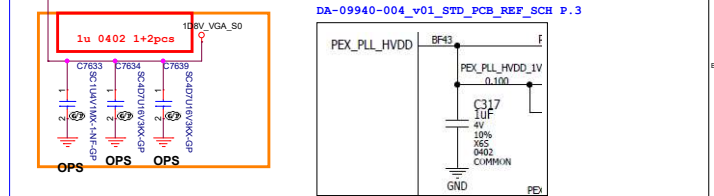
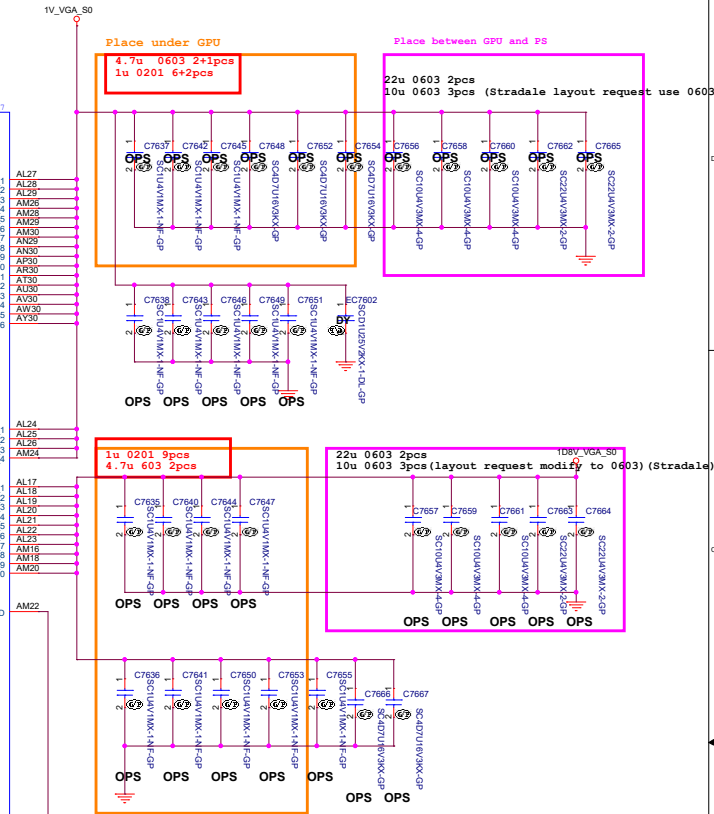
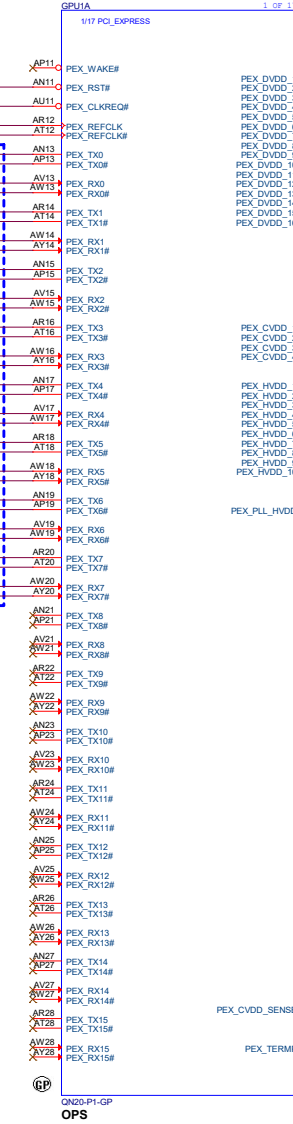
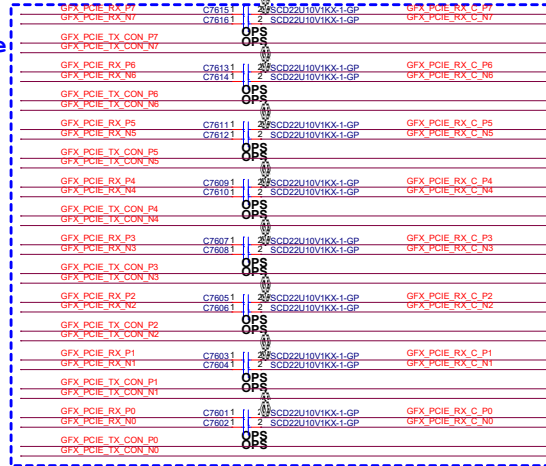
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>EXT IO (RSVD)</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 75 of	106

PEX\_CLKREQ# is an active-low, open-drain bi-directional signal. It must have a 10 kΩ pull-up to 1V8\_AON.



20200805  
reverse type



DG-09845-001\_v01 P.46

PEX_DVDD_x (x=1-12)	12	0.95V	6 x 1uF [0402 X6S]	3 x 10uF [0805]
PEX_CVDD_x (x=1-3)			2 x 4.7uF [0603 X6S]	2 x 22uF [0805]
PEX_PLL_HVDD	13	1.8V	9 x 1uF [0402 X6S]	3 x 10uF [0805]
			2 x 4.7uF [0603 X6S]	2 x 22uF [0805]

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Broadmor 15P

**DELL** Wistron Corporation  
21F, 88, Sec.1, Main Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

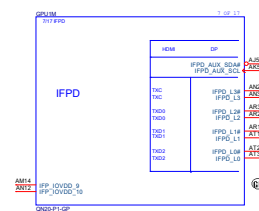
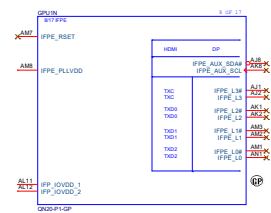
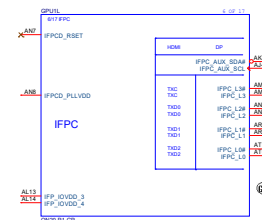
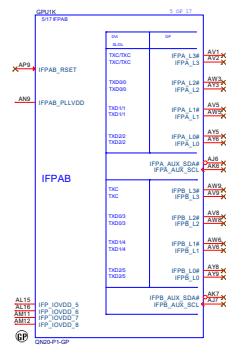
Part No: **076\_GPU (PEG 1/5\_QN20P1)**

Spec: **Broadmor 15 TGL-H**

Date: Monday, October 26, 2020

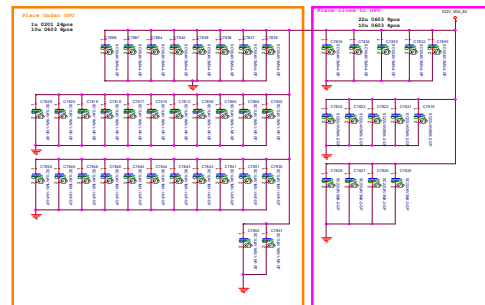
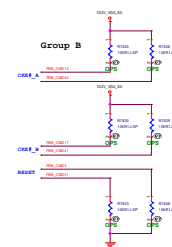
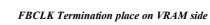
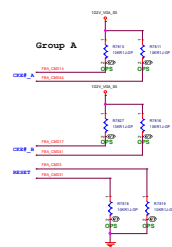
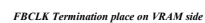
Rev: **X00**

```
Main Func = dGPU
```



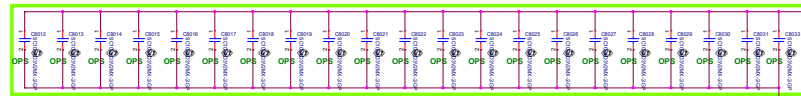
<https://vinafix.com>



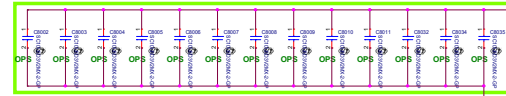




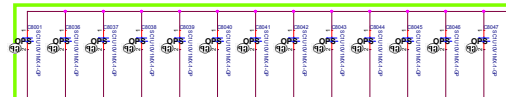
100U\*21  
Place under GPU



100U\*13  
Place under GPU



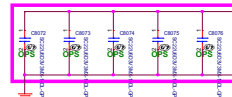
10U\*13  
Place under GPU



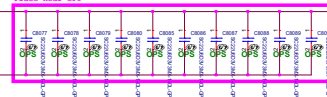
0.47U\*26  
Place under GPU



22U\*5  
Place near GPU



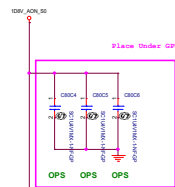
22U\*10  
Place near GPU



DA-09899-001\_v03 P.23

Table 2. NVDD Decoupling and Filtering

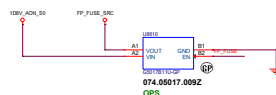
GPU	Capacitor Type	Footprint	Population		Location	
			GB5-128	GB5B-128		
NVDD Supply Net						
GB5-128	1 $\mu$ F	X6S	0402 or 0201W	13	13	Under GPU
GB5B-128	10 $\mu$ F	X6S	0603	34	34	Under GPU
	22 $\mu$ F	X6S	0805	15	15	Near GPU

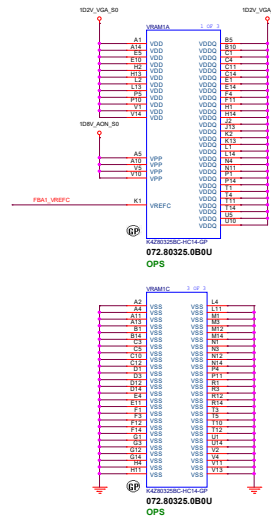
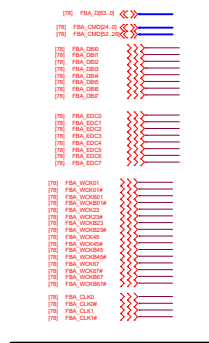


DA-09899-001\_v03 P.24

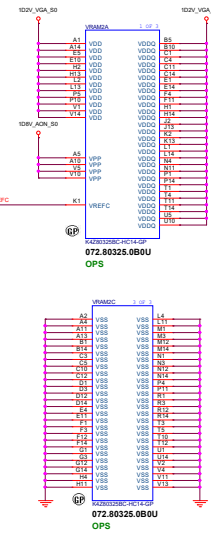
Table 8. TVS Decoupling

GPU	Capacitor Type	Footprint	Population		Location
			GB5-128	GB5B-128	
TVS Supply Rails					
GB5-128, GB5B-128	1.0 $\mu$ F	X6S	0402 or 0201W	2	Under GPU
	1.0 $\mu$ F	X6S	0402 or 0201W	3	Near GPU
	4.7 $\mu$ F	X6S	0403	3	Near GPU





Follow reference schematic



Follow reference schematic

#### 8.2.2.14 GDDR6 DRAM VREFC

GDDR6 DRAMs include an integrated VREFC (VREF for DQ07 and ADDR). Figure 8.8 illustrates use of the integrated VREFC for x16 mode GDDR6 DRAMs. Refer to the reference schematics for final component values.

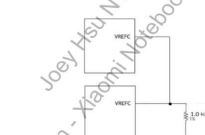
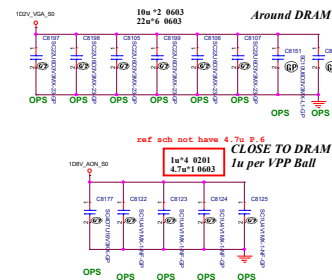
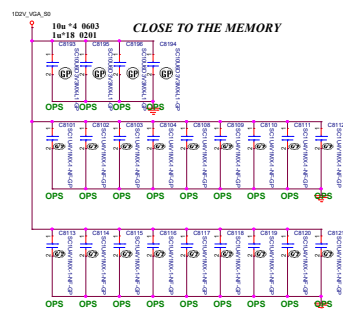


Figure 8.8 Use of Integrated VREFC for x16 Mode

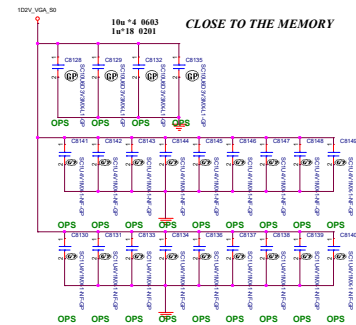
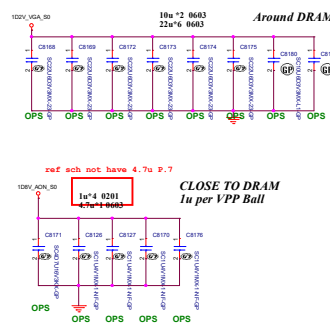
#### FOR VRAM1

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE



#### FOR VRAM2

PLACE 0201 1uF UNDER MEMORY AS MUCH AS POSSIBLE





5

4

3

2

1

D

D

C

C

B

B

A

A

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Broadmoor 15P

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>083_GPU (VRAM5,6 3/4)</b>					
Size A4		Document Number <b>Broadmoor 15 TGL-H</b>			Rev <b>X00</b>
Date: Monday, October 26, 2020		Sheet 83		of 106	

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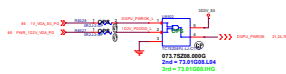
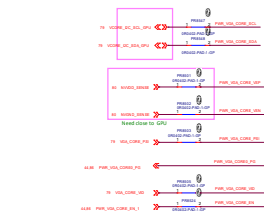
A

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Broadmoor 15P

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>084_GPU (VRAM7,8 4/4)</b>					
Size A4		Document Number <b>Broadmoor 15 TGL-H</b>			Rev <b>X00</b>
Date: Monday, October 26, 2020		Sheet 84		of 106	

00000723  
 000-000001 Power Multivibrator W552 OPS-M.  
 000-000001 Change to Power Multivibrator to Page 27



Pin	Power
Pin 1	12V
Pin 2	12V
Pin 3	12V
Pin 4	12V
Pin 5	12V
Pin 6	12V
Pin 7	12V
Pin 8	12V
Pin 9	12V
Pin 10	12V
Pin 11	12V
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Pin	Power
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Pin 100	12V

Pin	Power
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Pin 91	12V
Pin 92	12V
Pin 93	12V
Pin 94	12V
Pin 95	12V
Pin 96	12V
Pin 97	12V
Pin 98	12V
Pin 99	12V
Pin 100	12V

00000727  
 000-000001 Power Multivibrator W552 OPS-M.  
 000-000001 Change to Power Multivibrator to Page 27

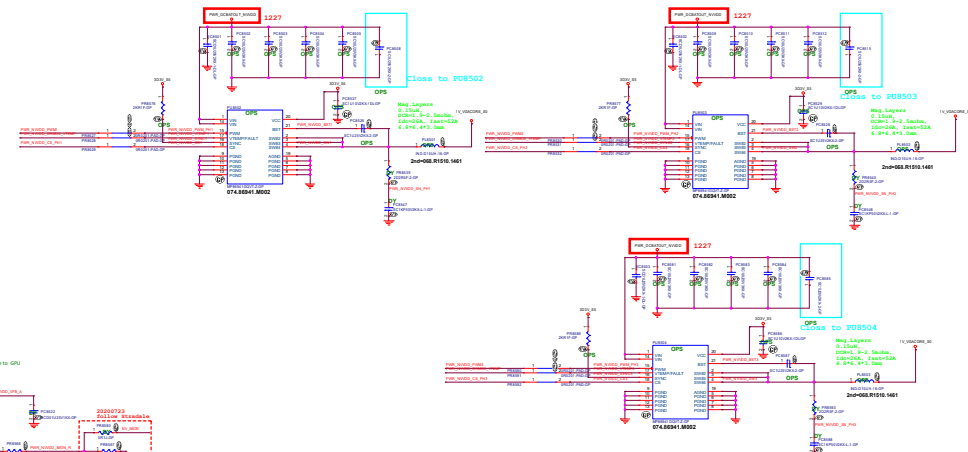
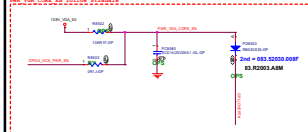


Table 7.8 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
Number of Voltage Levels N	level	160
PWM Frequency F <sub>pw</sub>	MHz	0.75
PWM Minimum Pulse Width T <sub>pw</sub>	ns	5.00
VID Transient Time T <sub>vid</sub>	us	<100
Component Value		
R1 (Ω)	KΩ	6.19
R2 (Ω)	KΩ	20.5
R3 (Ω)	KΩ	4.52
R4 (Ω)	KΩ	16.5
R5 (Ω)	KΩ	0.00
C	μF	0.3

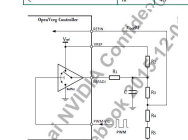


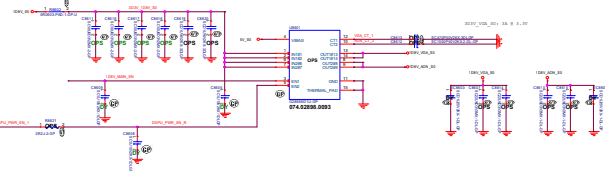
Table 7.9 PWM-VID Spec and Component Values

PWM-VID Specification	Unit	Config
V <sub>min</sub>	V	0.3
V <sub>max</sub>	V	1.3
V <sub>step</sub>	V	0.8
Voltage Step V <sub>step</sub>	mV	6.25
Number of Voltage Levels N	level	160
PWM Frequency F <sub>pw</sub>	MHz	0.75
PWM Minimum Pulse Width T <sub>pw</sub>	ns	5.00
VID Transient Time T <sub>vid</sub>	us	<100
Component Value		
R1 (Ω)	KΩ	6.19
R2 (Ω)	KΩ	20.5
R3 (Ω)	KΩ	4.52
R4 (Ω)	KΩ	16.5
R5 (Ω)	KΩ	0.00
C	μF	0.3

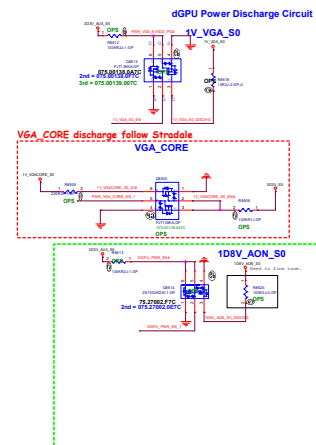
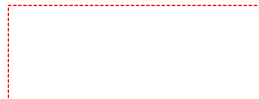


Main Func = dGPU

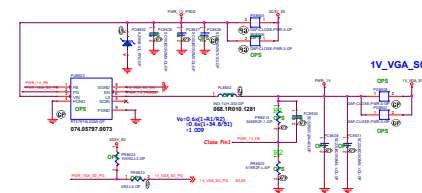
(DP-07154-001 Rev03) Power Up Sequence  
 1. 3V with 0V0V0 (VGA\_CORE) with 0V0V0 (VGA\_S0) with 0V0V0 (VGA\_S0)  
 3D3V\_S0 to 3V3\_AON\_S0 and 3D3V\_VGA\_S0



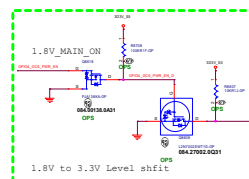
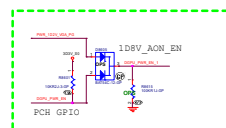
20200807  
 DGPU\_PWR\_EN follow Straddle



RT5797 for 1V\_VGA\_S0

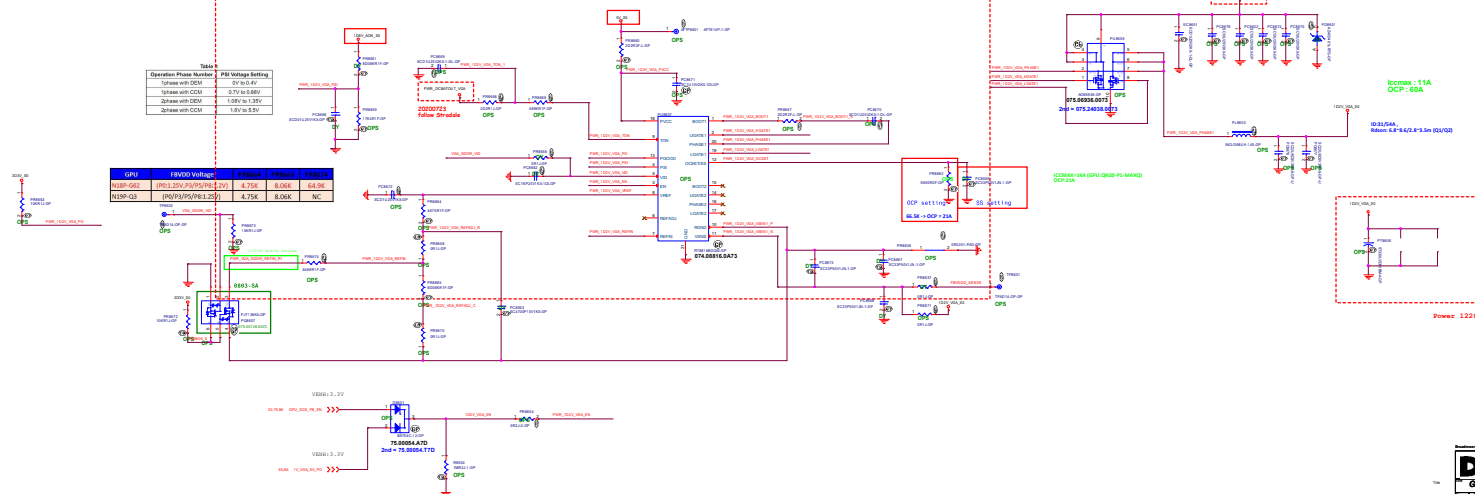


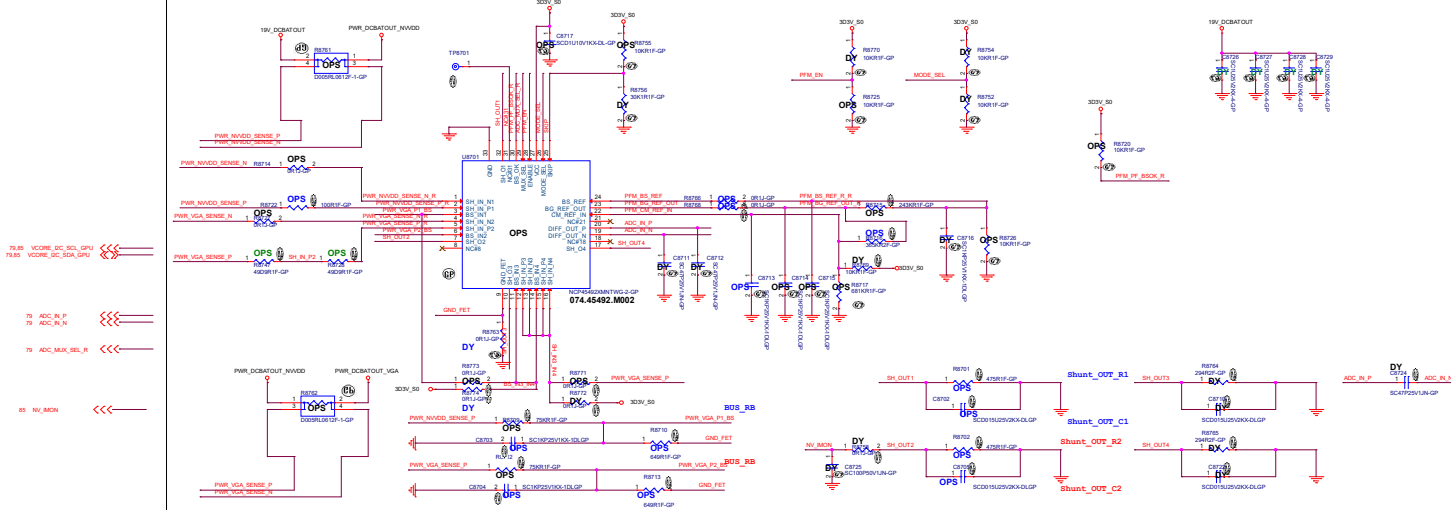
20200805  
 1D8V\_MAIN\_EN follow Straddle



Operation Phase Number	PSM Voltage Setting
1. Standby with CPU	0.7V to 0.7V
2. Standby with CPU	0.7V to 0.7V
3. Standby with CPU	0.7V to 0.7V
4. Standby with CPU	0.7V to 0.7V

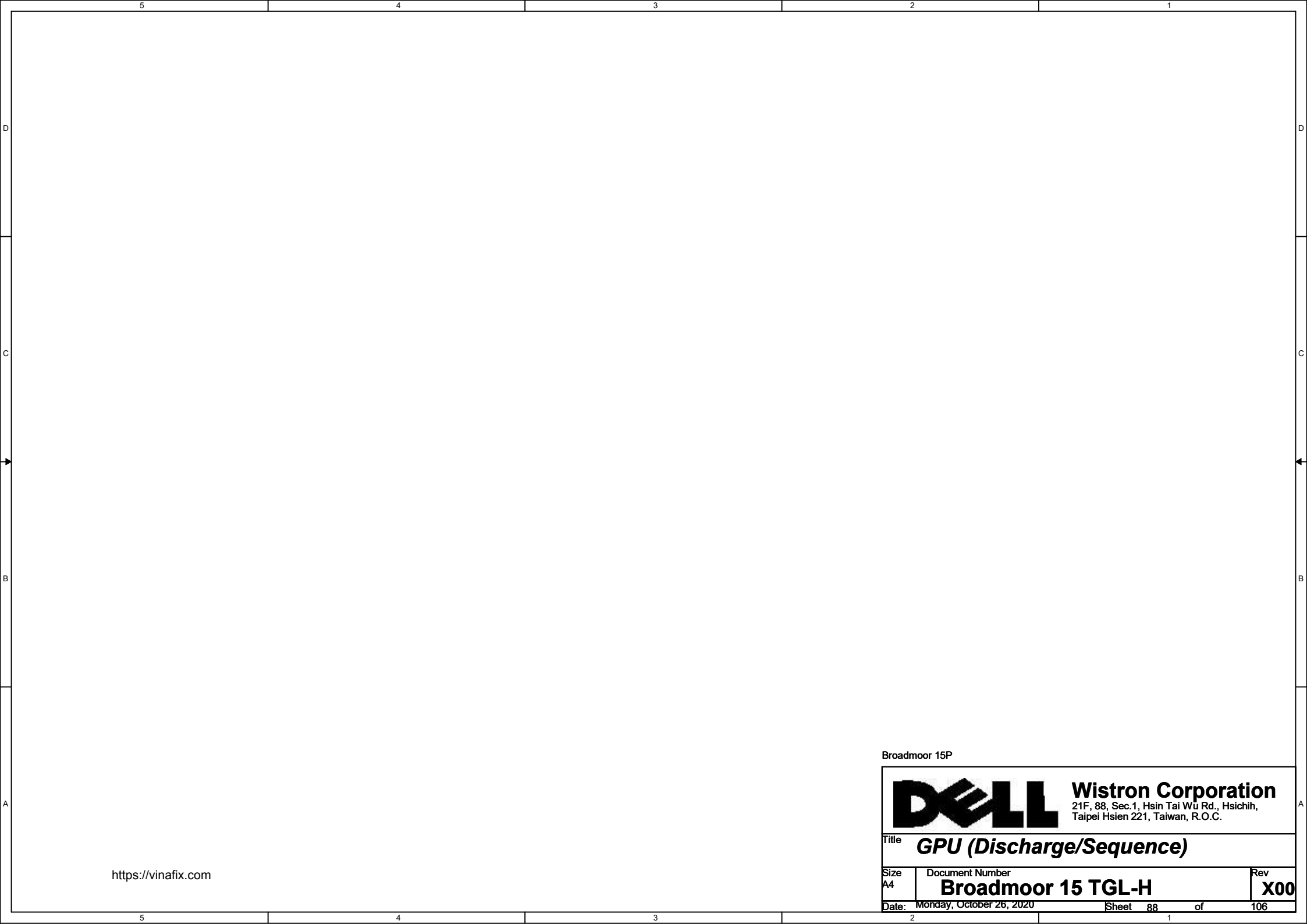
GPU	VRMS Voltage
VRMS0	1.0V to 1.0V
VRMS1	1.0V to 1.0V
VRMS2	1.0V to 1.0V
VRMS3	1.0V to 1.0V






discharge circuit on page 86

Vcore\_OVP circuit on page 44

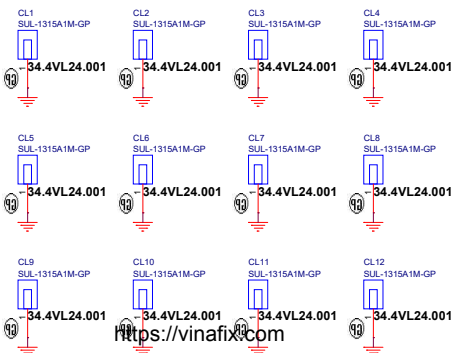
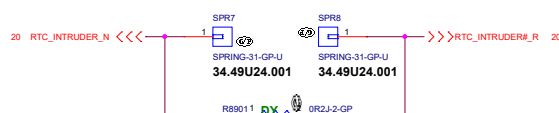
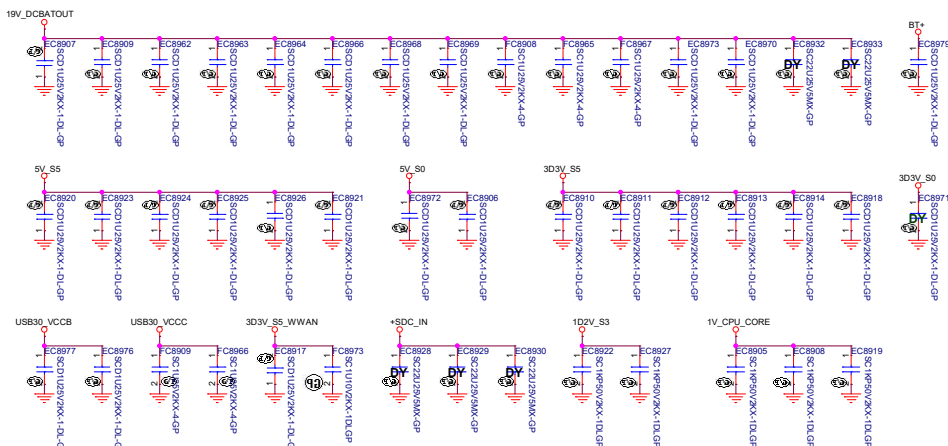


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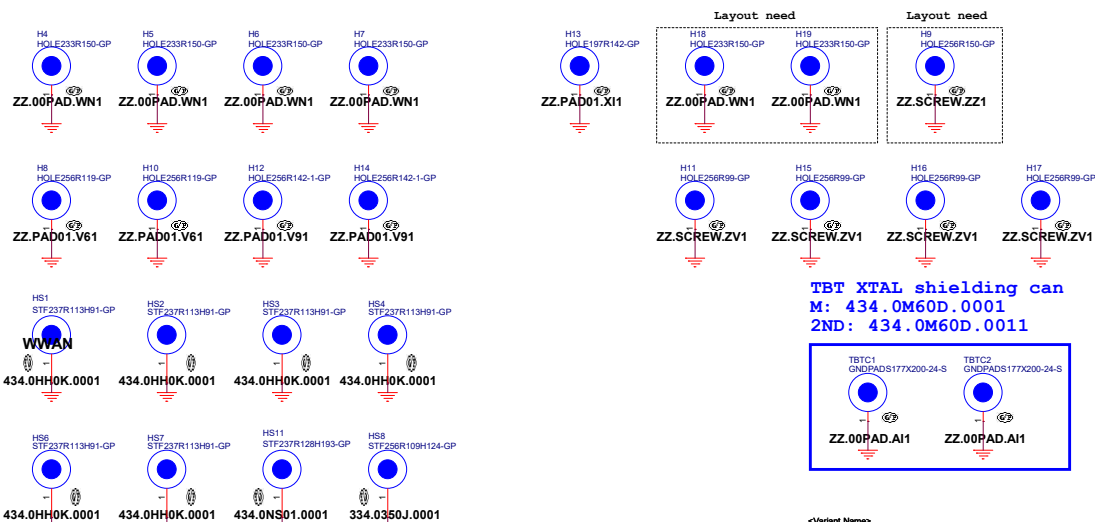
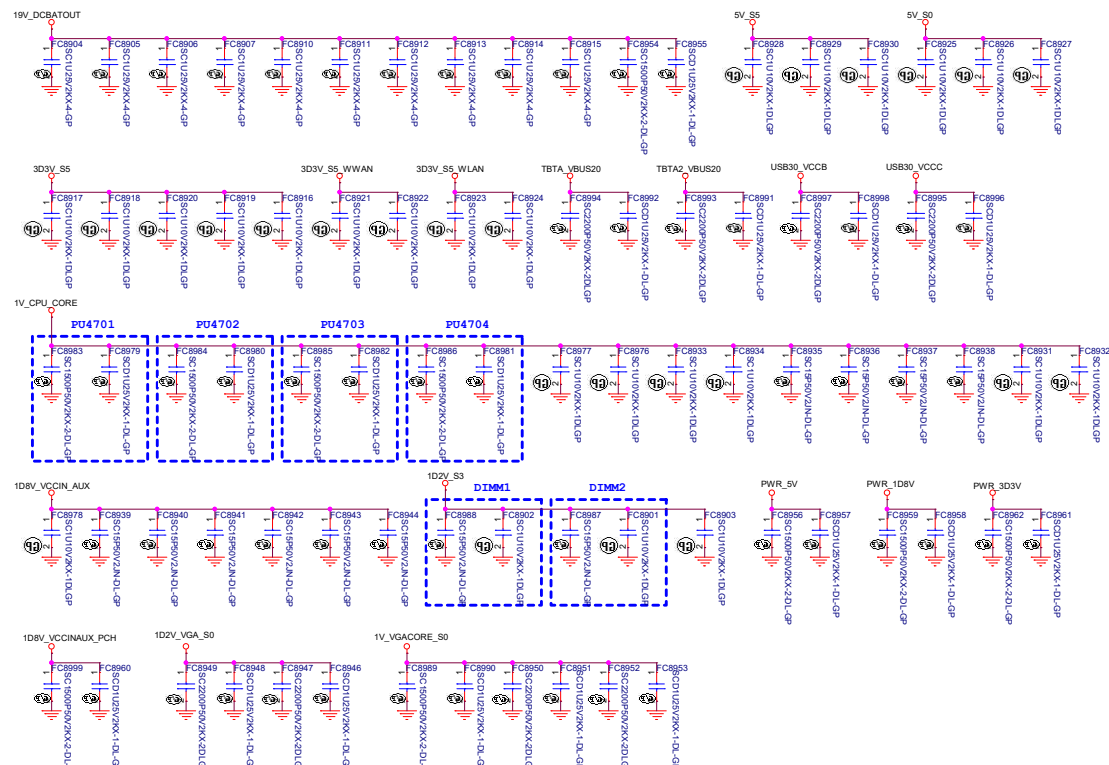
Broadmoor 15P

			<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title <b>GPU (Discharge/Sequence)</b>					
Size A4		Document Number <b>Broadmoor 15 TGL-H</b>			Rev <b>X00</b>
Date: Monday, October 26, 2020		Sheet 88		of 106	

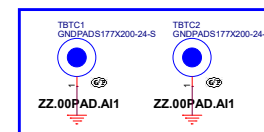
**Main Func = EMC/ RF**



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TBT XTAL shielding can  
M: 434.0M60D.0001  
2ND: 434.0M60D.0011



5	4	3	2	1
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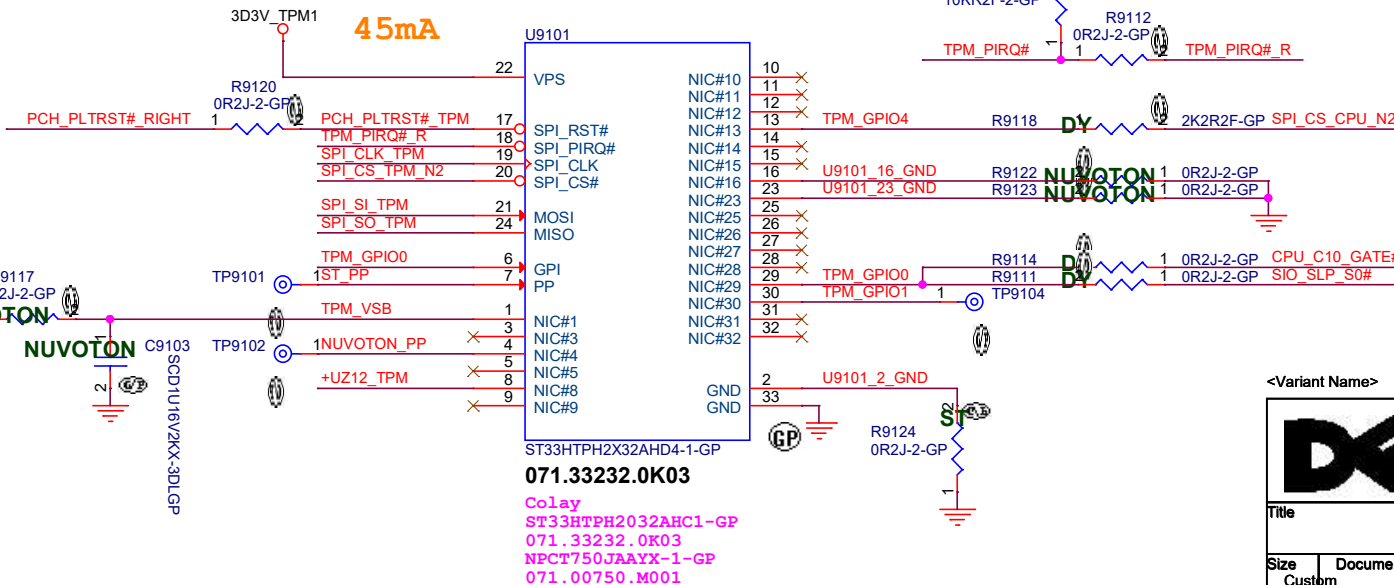
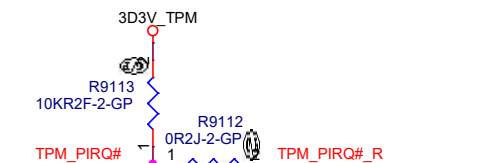
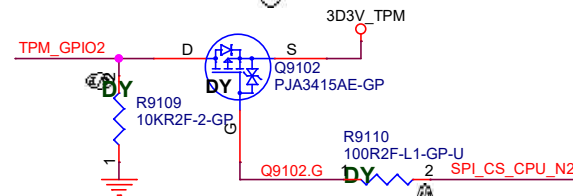
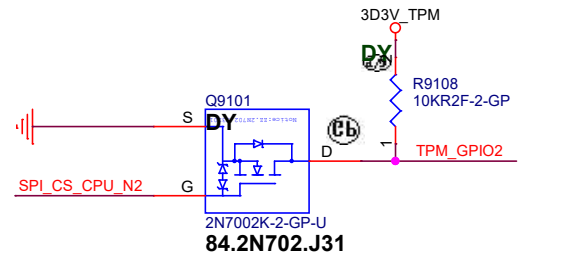
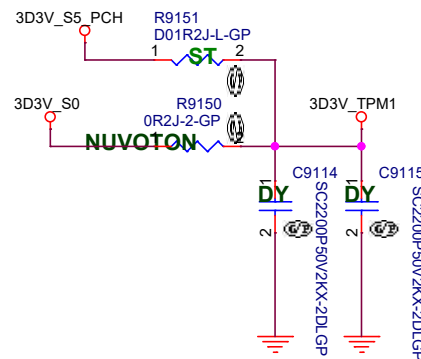
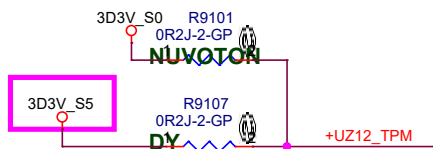
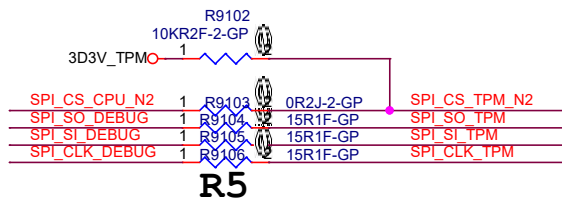
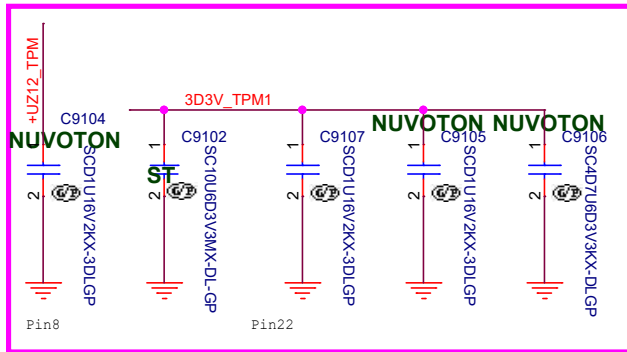
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>INT IO (RSVD) (NFC)</b>		
Size A4	Document Number	Rev <b>X01</b>
Date: Monday, October 26, 2020	Sheet 90 of	106

# Main Func = TPM

20 TPM\_PIRQ#  
20,68 SIO\_SLP\_S0#  
20,33,61,62,79,97 PCH\_PLTRST#\_RIGHT

24,25,68 SPI\_CLK\_DEBUG  
24,25,68 SPI\_SI\_DEBUG  
24,25,68 SPI\_SO\_DEBUG  
18,96 SPI\_CS\_CPU\_N2  
21,40 CPU\_C10\_GATE#



Close U9101 (p.91)

96 SPI\_CLK\_TPM  
96 SPI\_SI\_TPM  
96 SPI\_CS\_TPM\_N2

<Variant Name>



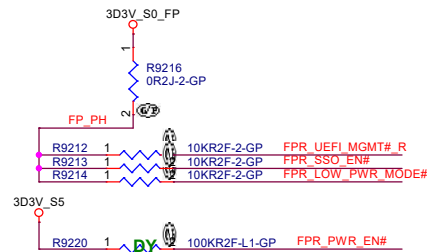
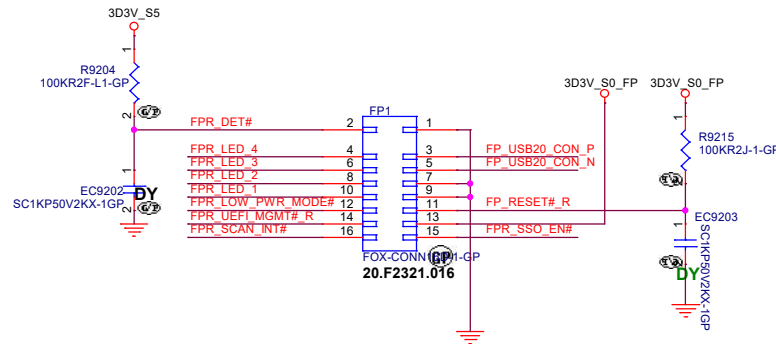
Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

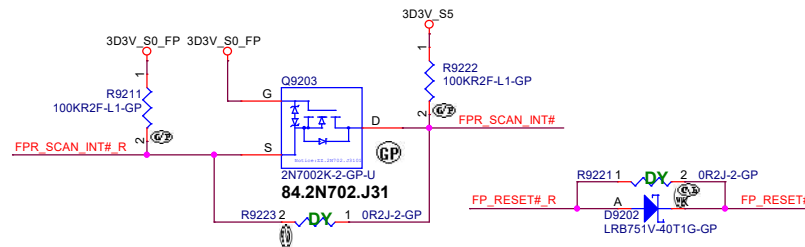
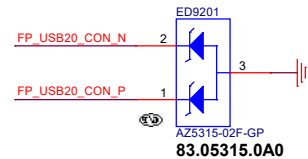
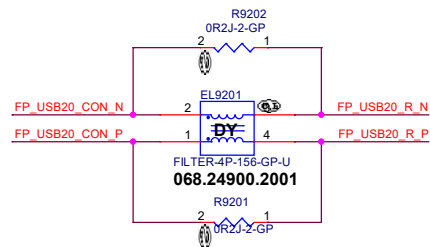
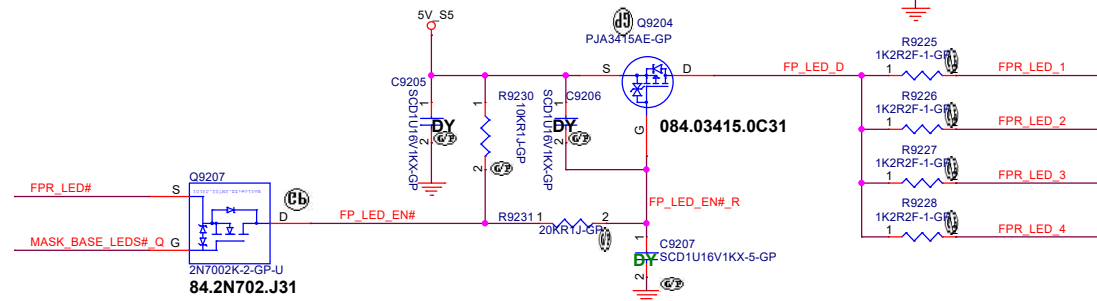
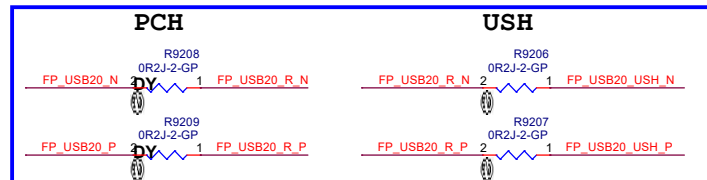
Title			INT IO (TPM)
Size	Document Number	Rev	
Custom		X01	
Date:	Monday, October 26, 2020	Sheet	91 of 106

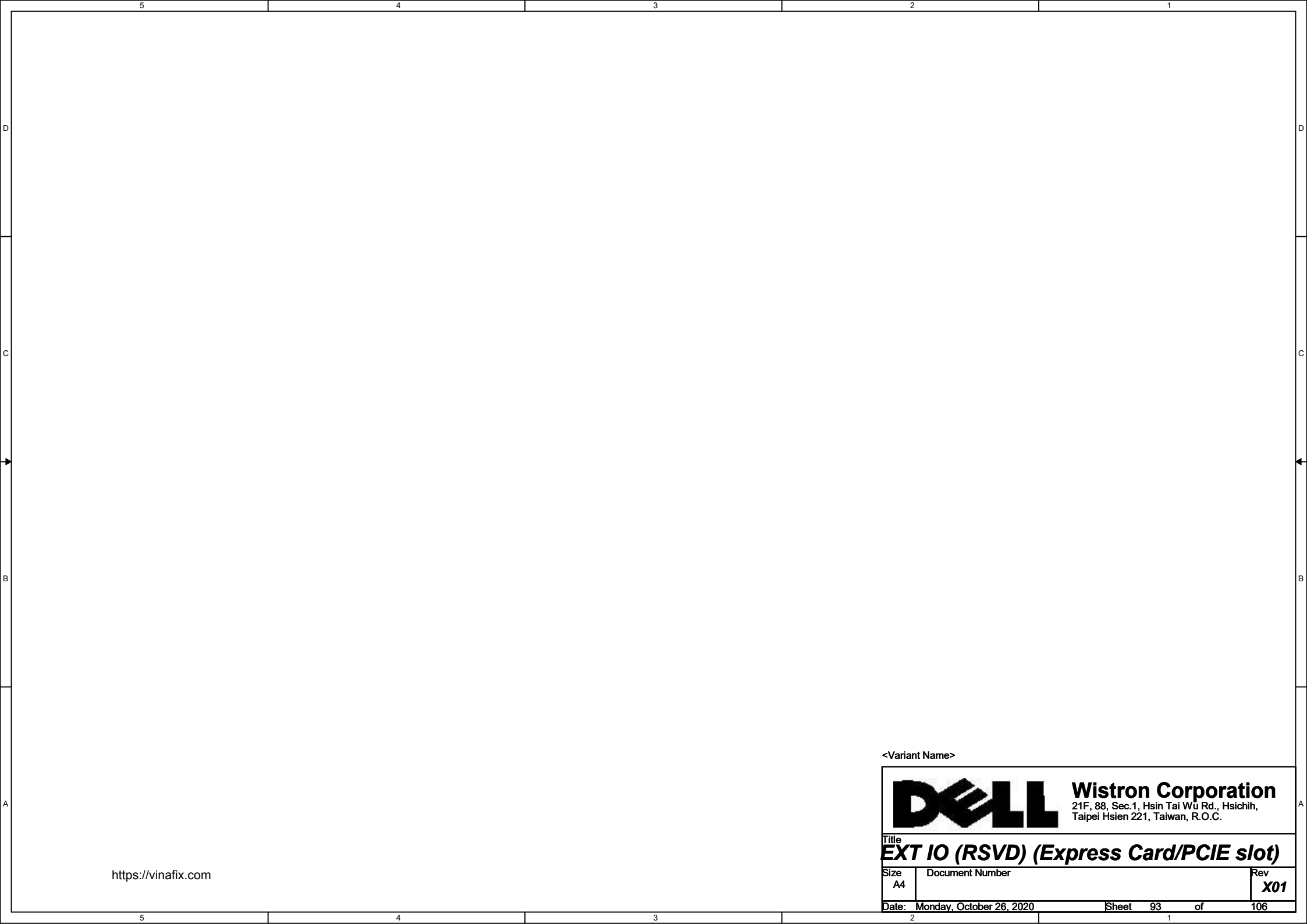
# Main Func = Finger Printer

18 FP\_USB20\_P <<<>>>  
 18 FP\_USB20\_N <<<>>>  
 24,64 FPR\_DET# <<<<<<  
 66 FP\_USB20\_USH\_N <<<>>>  
 66 FP\_USB20\_USH\_P <<<>>>  
 24 FPR\_PWR\_EN# >>>>>>  
 24,66 FPR\_SCAN\_INT# <<<<<<  
 24 FPR\_SSO\_EN# >>>>>>  
 24 FPR\_UEFI\_MGMT#\_R >>>>>>  
 24 FPR\_LOW\_PWR\_MODE# >>>>>>  
 66 FP\_RESET# >>>>>>  
 24 FPR\_LED# <<<<<<  
 64 MASK\_BASE\_LEDS#\_Q >>>>>>




Try to co-lay





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<Variant Name>


		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>EXT IO (RSVD) (Express Card/PCIE slot)</b>		
Size A4	Document Number	Rev <b>X01</b>
Date: Monday, October 26, 2020	Sheet 93 of	106



5	4	3	2	1
D				
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<https://vinafix.com>


<Variant Name>

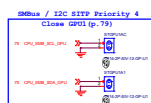
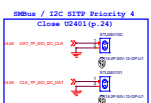
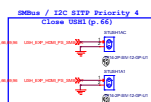
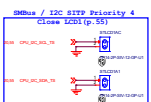
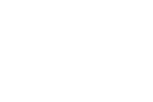
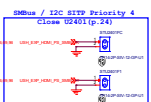
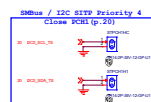
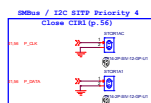
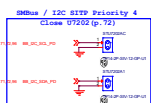
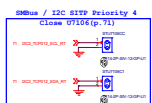
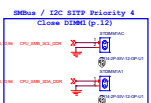
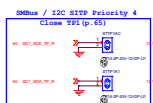
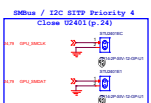
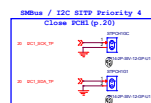
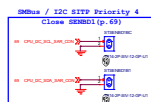
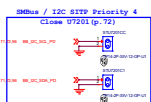
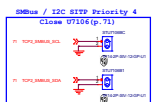
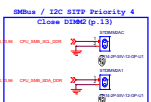
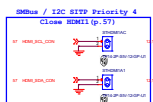
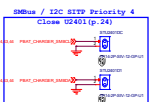
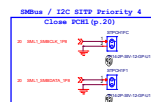
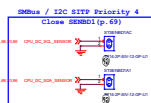
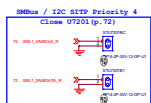
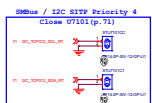
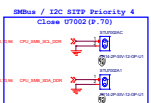
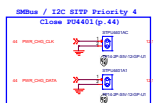
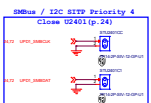
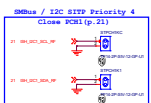
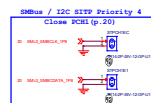
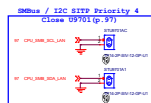
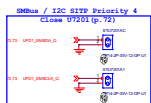
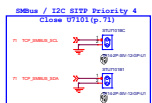
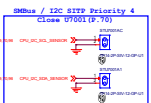
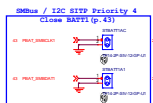
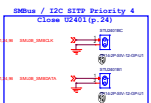
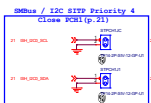
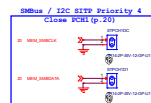
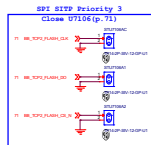
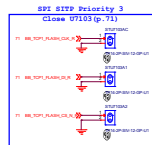
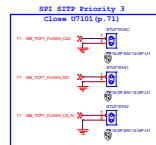
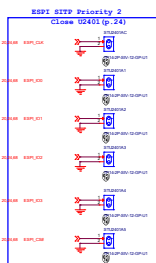
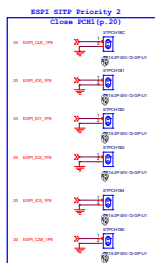
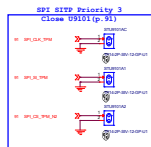
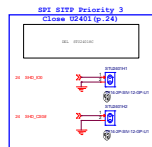
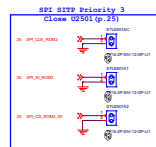
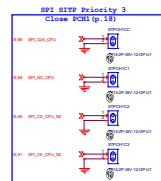
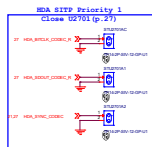
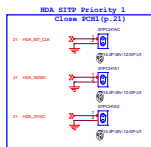
		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>EXT IO (RSVD) (Smart Card/COM/PS2)</b>		
Size A4	Document Number	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 94 of 106

5	4	3	2	1
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C				
B				
A				

<https://vinafix.com>

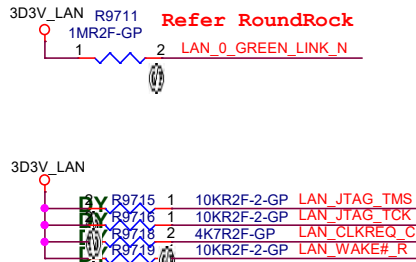
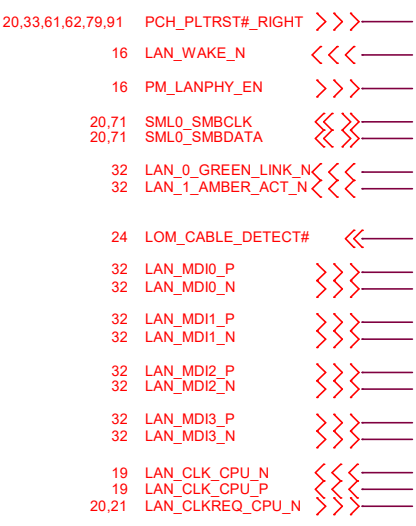
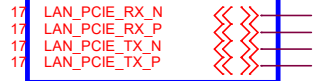
<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>EXT IO (RSVD) (Docking/LPT)</b>		
Size A4	Document Number	Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 95 of 106



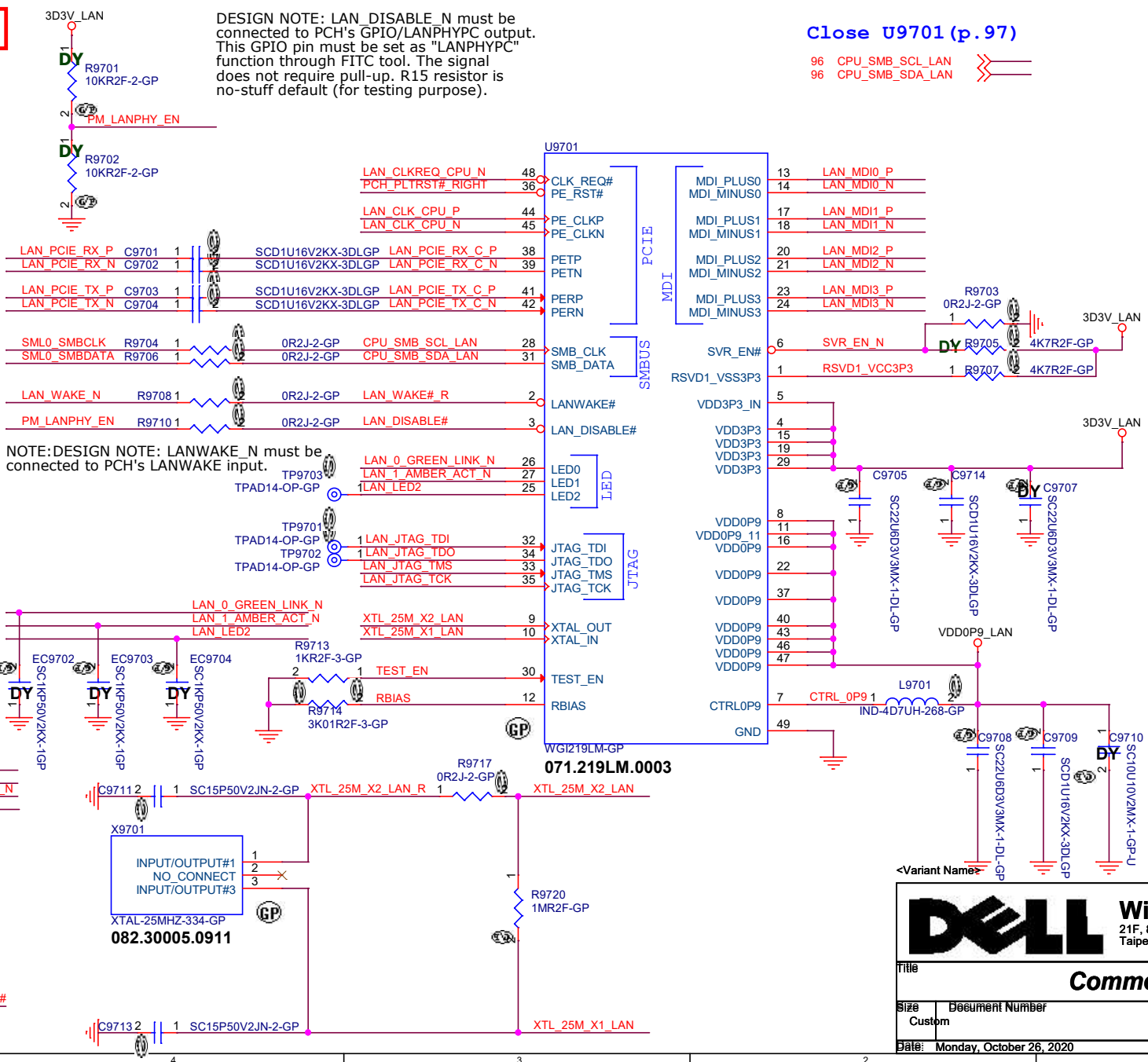
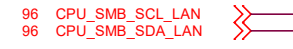
# Main Func = LAN


## LAN



DESIGN NOTE: LAN\_DISABLE\_N must be connected to PCH's GPIO/LANPHYC output. This GPIO pin must be set as "LANPHYC" function through FITC tool. The signal does not require pull-up. R15 resistor is no-stuff default (for testing purpose).

Close U9701(p.97)





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**Commercial (Intel LAN)**

Size	Document Number	Rev
Custom		<b>X01</b>
Date:	Monday, October 26, 2020	Sheet 97 of 106

5	4	3	2	1
D				
C				
B				
A				

<https://vinafix.com>

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title <b>Commercial (LAN Switch)</b>		
Size A4	Document Number	Rev <b>X01</b>
Date: Monday, October 26, 2020	Sheet 98 of	106

# Main Func = Debug

6 CPU\_CFG3 <<<<—  
  
6 VCCST\_PWRGD <<<<—  
4,99 CPU\_EAR <<<<—  
20,63,71 PCH\_PLTRST#\_LEFT <<<<—  
11,20 DBG\_PMODE <<<<—  
6,17 CPU\_JTAG\_PRDY\_N <<<<—  
16,17,24,64 RSMRST#\_KBC <<<<—  
68 XDP\_SPI\_WP\_CPU <<<<—  
40 XDP\_OVERRIDE# <<<<—  
6,17 CPU\_JTAG\_PREQ\_N <<<<—  
4,99 CPU\_EAR <<<<—

20 PCH\_JTAG\_TCK <<>>—  
6 CPU\_JTAG\_TRST\_N <<>>—  
6 CPU\_JTAG\_TCK <<>>—  
6 CPU\_JTAG\_TDI <<>>—  
6 CPU\_JTAG\_TDO <<>>—  
6 CPU\_JTAG\_TMS <<>>—

19 PCH\_JTAG\_TRST\_N <<>>—  
20 PCH\_JTAGX <<>>—  
20 PCH\_JTAG\_TMS <<>>—  
20 PCH\_JTAG\_TDO <<>>—  
20 PCH\_JTAG\_TDI <<>>—

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PCH\_PLTRST#\_LEFT 1 2 1KR1F-GP  
DBG\_PMODE R9923 1 2 0R1J-GP XDP\_DBG\_PMODE\_RST#  
R9922 DEBUG

CPU\_JTAG\_PRDY\_N 1 2 0R1J-GP XDP\_PRDY#  
R9921 DEBUG

VCCST\_PWRGD 1 2 1KR1F-GP  
RSMRST#\_KBC R9927 1 2 0R1J-GP XDP\_RSMRST#  
R9920 DEBUG

XDP\_SPI\_WP\_CPU 1 2 0R1J-GP XDP\_PRESENT1#  
R9919 DEBUG

CPU\_CFG3 1 2 1K5R1F-GP  
XDP\_OVERRIDE# R9930 1 2 0R1J-GP XDP\_PRESENT2#  
R9918 DEBUG

CPU\_JTAG\_PREQ\_N 1 2 0R1J-GP XDP\_JTAG\_PREQ#  
R9917 DEBUG

PCH\_JTAG\_TRST\_N 1 2 0R1J-GP XDP\_JTAG\_TRST#  
CPU\_JTAG\_TRST\_N R9905 1 2 0R1J-GP  
R9904 DEBUG

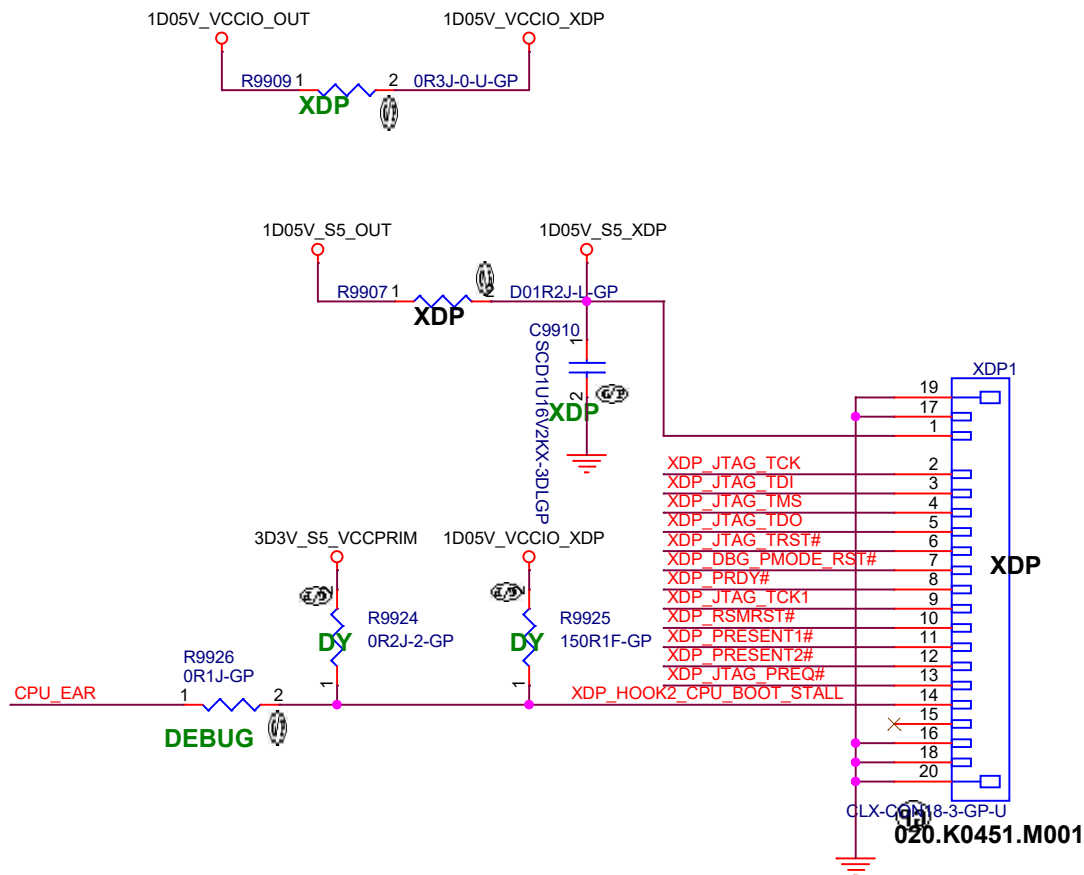
PCH\_JTAG\_TDI 1 2 0R1J-GP XDP\_JTAG\_TDI  
CPU\_JTAG\_TDI R9911 1 2 0R1J-GP  
R9906 DEBUG

PCH\_JTAG\_TDO 1 2 0R1J-GP XDP\_JTAG\_TDO  
CPU\_JTAG\_TDO R9912 1 2 0R1J-GP  
R9908 DEBUG

PCH\_JTAG\_TMS 1 2 0R1J-GP XDP\_JTAG\_TMS  
CPU\_JTAG\_TMS R9913 1 2 0R1J-GP  
R9910 DEBUG

PCH\_JTAGX 1 2 0R1J-GP XDP\_JTAG\_TCK  
CPU\_JTAG\_TCK R9914 1 2 0R1J-GP  
R9931 DEBUG

PCH\_JTAG\_TCK 1 2 0R1J-GP XDP\_JTAG\_TCK1  
R9916 DEBUG



<Variant Name>



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Title

**Debug (XDP debug)**

Size  
A4

Document Number

**Broadmoor 15 TGL-H**

Rev  
**X01**

Date: Monday, October 26, 2020

Sheet 99 of 106

# Table of Content

## RESISTOR

Symbol name	Value	Tolerance  (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating  0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size  2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603


The naming rule is value + R + size + tolerance  
 For the value, it can be read by the number before R. (R means resistor)  
 For the tolerance, it can be read from the last letter.  
 For the rating, we don't show on the symbol name.  
 For the size, R2=>0402, R3=>0603, R5=>0805,....

## CAPACITOR

Symbol name	Value	Tolerance  (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size  2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is  
 Capacitor type + value + rating + size + tolerance + material  
 SCD1U10V2MX-1  
 SC=> SMT Ceremic, TC=> POS cap or SP cap  
 D1U => 0.1uF  
 10V => the voltage rating is 10V  
 2=> 0402, 3=>0603, 5=>0805  
 M=>tolerance M, K, Z  
 X=> X7R/X5R, Y=> Y5V  
 -1 => symbol version, nonsense to EE characteristic

<Variant Name>



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Title

Table of Content

Size

A4

Document Number

Rev

X01

Date

Monday, October 26, 2020

Sheet

100

of

106


Change notes -

DATE	VERSION	DATE	Page	Modify List	OWNER
	X00	3/10	5.12.13	DDR4 Non-Interleaved Type change to Interleaved Type	
	X00	3/10	40	VCCST_EN add colay RUN_ON_R ( R74014 & R74015 )	
	X00	3/12	18	Add WWAN USB3 port4	
	X00	3/12	17	Change WWAN pcie to PORT1	
	X00	3/12	17	Change WLAN pcie to PORT2	
	X00	3/12	17	Change SD cardreader pcie to PORT3	
	X00	3/12	17	Change SSD pcie to PORT9.10.11.12	
	X00	3/12	18	Change BT USB2 to PORT1	
	X00	3/12	18	Change CCD USB2 to PORT3	
	X00	3/12	18	Change CV3 USB2 to PORT5	
	X00	3/12	18	Change WWAN USB2 to PORT7	
	X00	3/12	18	Change Type-C 1 USB2 to PORT8	
	X00	3/12	18	Change FPR USB2 to PORT10	
	X00	3/12	18	Change Type-A 1 USB2 to PORT11	
	X00	3/12	18	Change Type-C 2 USB2 to PORT12	
	X00	3/12	18	Change Type-A 2 USB2 to PORT12	
	X00	3/12	4	Change HDMI net name	
	X00	3/12	63	Change SSD1 net name to PCIE	
	X00	3/12	76	Add GFX PCIE 4~7	
	X00	3/16	5.12.13	DDR4 add ECC	
	X00	3/17		GPU change to N18S	
	X00	3/18	40	power sequence follow DIONYSOS_TGLH	
	X00	3/23	10,44~54,86.87	change power SCH	
	X00	3/23	06.99	Change BPM net name	
	X00	3/23	07.08	Change power net name	
	X00	3/27		Set SSID	
	X00	3/27	22.25.40	Add DS5 SCH	
	X00	3/30		DDR4 Type change to Non-Interleaved Type	
	X00	3/30	76~86	GPU change to N18P	
	X00	4/14	3.17.63	SSD1.SSD2 change	
	X00	4/14	73	U7302 change to TS3DS10224	

X00	4/15	72	Change PD I2C
X00	4/21	18	ADD SPI follow SP15
X00	4/21	20.21	DEL RN2101 ADD RN2012
X00	4/21	20	DEL RN2005
X00	4/21	20	DEL Q2004 & RN2102 ADD RN2013
X00	4/21	21	ADD R2103~R2106
X00	4/21	20	Del Q2002 Q2001 Q2003 RN2008
X00	4/29	3.17.63	SSD1.SSD2 change
X00	5/4	80~86	GPU cap change to X6S

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Title

Change History

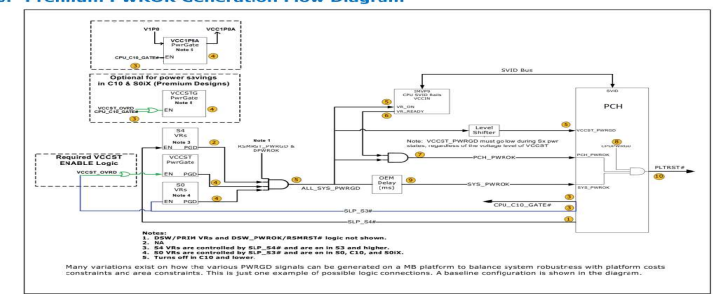
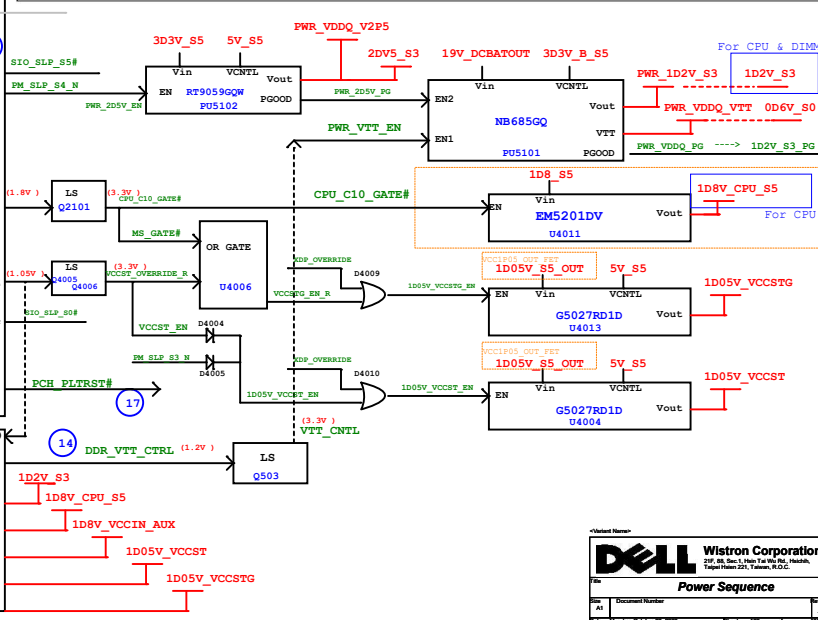
Size  
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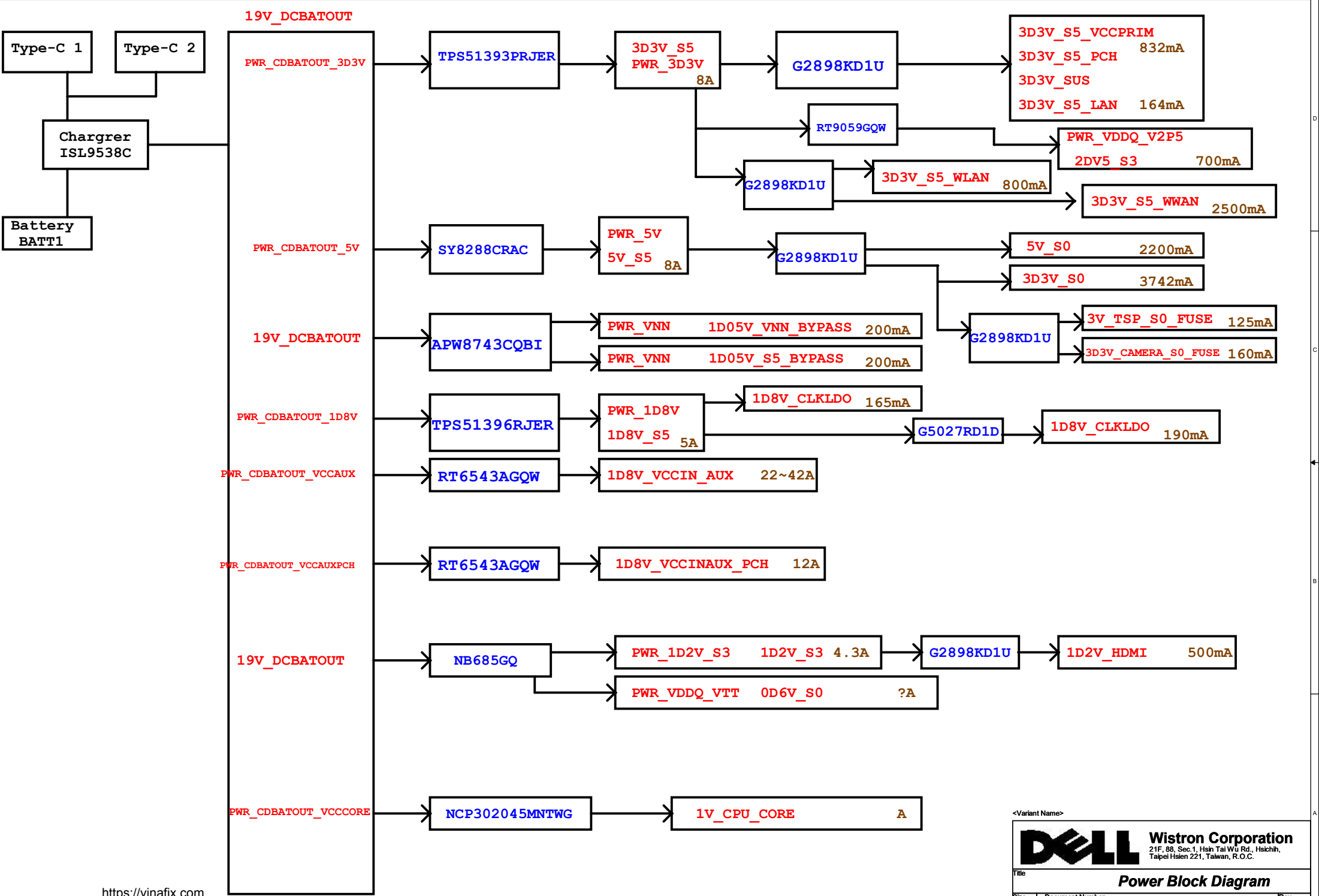
Document Number

Rev  
X01

Date: Monday, October 26, 2020Sheet 101 of 108




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<Variant Name>



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Title: **Power Block Diagram**

Size: A3	Document Number:	Rev: <b>X01</b>
Date: Monday, October 26, 2020	Sheet: 103 of 106	

## TGL\_H



0x14

## TGL H



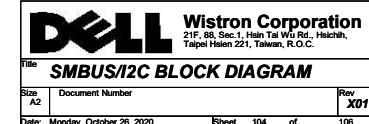
Pin Name	Pin #	Type	Op Mode	Name and Function
SMB_CLK	28	Q/I	Bi-dir	<p>SMBus clock.</p> <p>Pull this signal up to 1.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).</p>
SMB_DATA	31	Q/I	Bi-dir	<p>SMBus data.</p> <p>Pull this signal up to 1.3 Vdc (auxiliary supply) through a 499Ω resistor (while in Sx mode).</p>

**Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship**

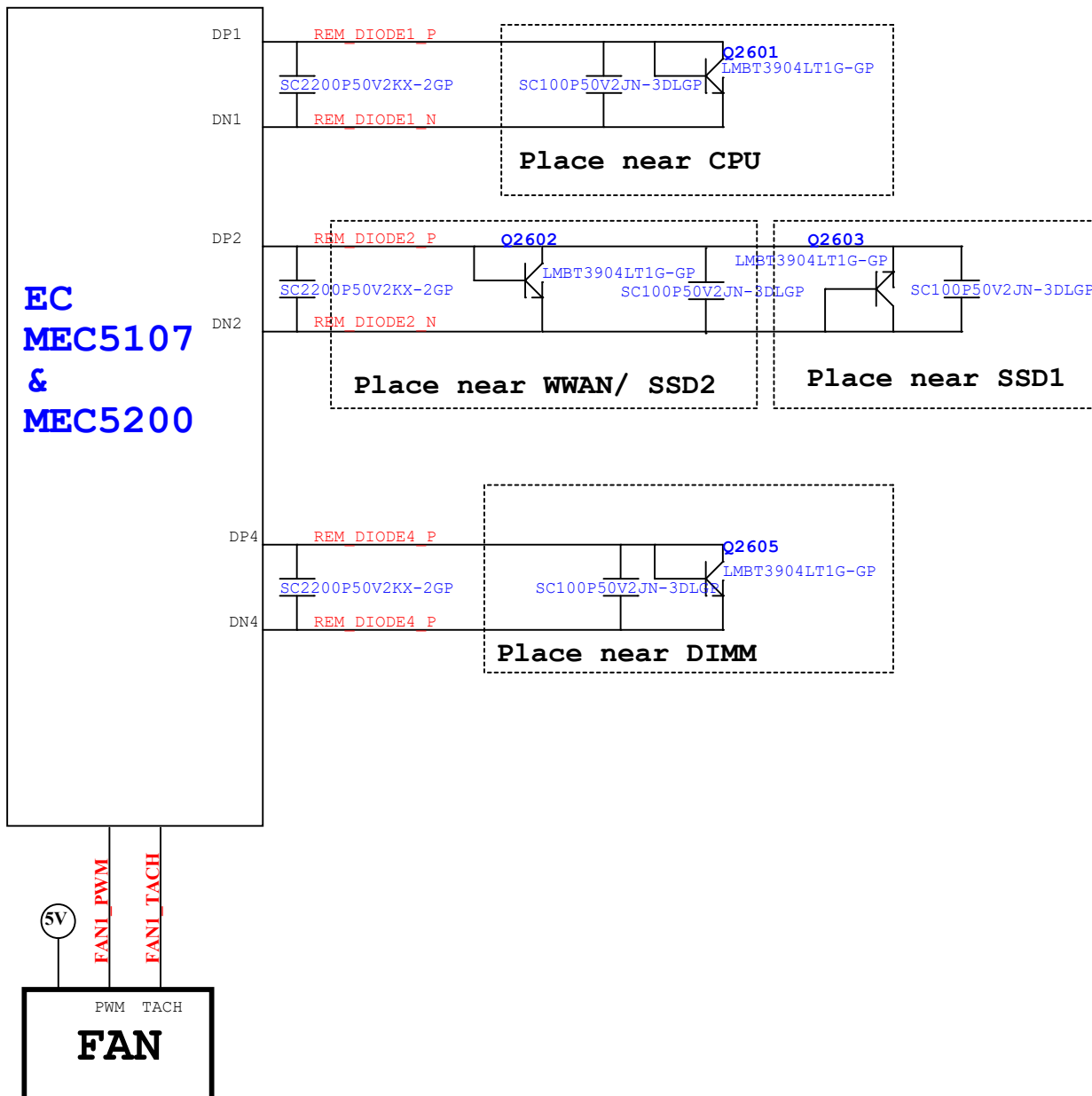
Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance ( $C_b$ )	External Pull-up	PCH Pull Down Strength (Refer E05)
Up to 450 pF	2.2kΩ	1000
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance ( $C_b$ )	External Pull-up	PCH Pull Down Strength

	Up to 100µF	2.2KΩ	1000
	Up to 200µF	1.5KΩ	
	Up to 300µF	1KΩ	
	Up to 400 µF	680Ω	
<b>Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings</b>			
<b>Total Bus Capacitance (C<sub>L</sub>)</b>		<b>External Pull-up</b>	<b>PCH Pull Down Strength</b>
	Up to 50pF	2.2KΩ	1000
	Up to 100pF	1.2KΩ	
	Up to 200pF	960Ω	
	Up to 300pF	390Ω	
	Up to 400 pF	270Ω	420

<Variant Name>

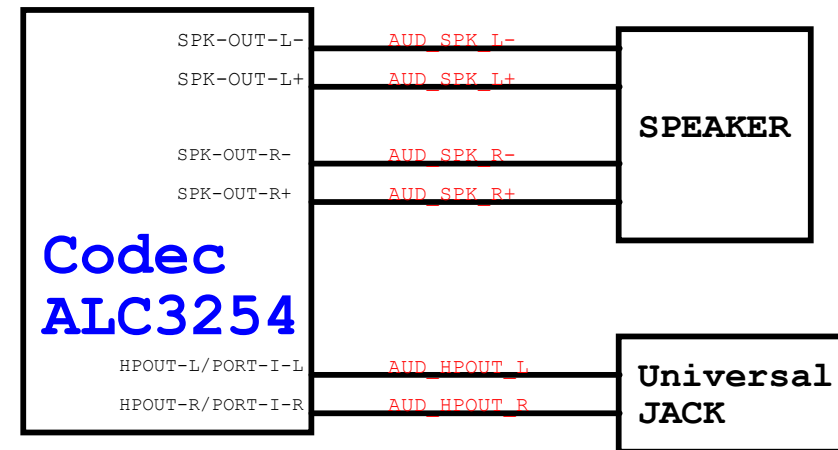


# Thermal Block Diagram



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# Audio Block Diagram




<Variant Name>

<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>THERMAL/AUDIO BLOCK DIAGRAM</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020		Sheet 105 of	106

5	4	3	2	1
D				
C				
B				
A				

<Variant Name>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>CLK Block</b>			
Size A4	Document Number		Rev <b>X01</b>
Date: Monday, October 26, 2020	Sheet	106	of 106